Exhibit 1

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
61/435,278	01/22/2011		220	ECC-0452-US		

CONFIRMATION NO. 5581

FILING RECEIPT

31864
VIASAT, INC.
C/O Stacy Nguyen
PATENT DEPARTMENT
6155 EL CAMINO REAL
CARLSBAD, CA 92009

Date Mailed: 03/15/2011

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

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If Required, Foreign Filing License Granted: 03/11/2011
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/435,278**
Projected Publication Date: None, application is not eligible for pre-grant publication
Non-Publication Request: No
Early Publication Request: No
Title

High Rate Optical Communication

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[Exhibit 1-2]

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Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (11-08)
Approved for use through 09/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Provisional Application for Patent Cover Sheet

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c)

Inventor(s)

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Yuri		Zelensky	Cleveland	OH	US

All Inventors Must Be Listed – Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. — Add

Title of Invention	High Rate Optical Communication
Attorney Docket Number (if applicable)	ECC-0452-US

Correspondence Address

Direct all correspondence to (select one):

◉ The address corresponding to Customer Number	○ Firm or Individual Name

EFS - Web 1.0.1

[Exhibit 1-5]

Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (11-08)
Approved for use through 09/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Customer Number	31864

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.
◉ No.
○ Yes, the name of the U.S. Government agency and the Government contract number are:

Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (11-08)
Approved for use through 09/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Entity Status

Applicant claims small entity status under 37 CFR 1.27

◯ Yes, applicant qualifies for small entity status under 37 CFR 1.27

◉ No

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Signature

Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Dr. Charles Nicholas Pateros #50,677/			Date (YYYY-MM-DD)	2011-01-22
First Name	Charles	Last Name	Pateros	Registration Number (If appropriate)	50677

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PROVISIONAL APPLICATION FOR PATENT

TITLE: High Rate Optical Communication
INVENTORS: Sameep Dave, Fan Mo, Bill Thesling, Matt Nimon, Lawrence Esker, Yuri Zelensky
DOCKET: ECC-0452-US
DATE: January 22, 2011

Cross Reference to Related Applications

NOT APPLICABLE

Federal Research Statement

NOT APPLICABLE

Background of Invention

While fiber optic channels are considered very good for data transmission, this assumption breaks down at high rates such as 40-100 Gbps and beyond. At these rates, new modulation, demodulation and error correction techniques are required.

Summary of Invention

Enabling technologies for the successful transmission and reception of high rate digital signals over optical channels are presented. Implementation strategies for low-complexity, easily realizable systems are also disclosed. Although the solutions are presented in the context of an optical transport environment, the techniques and embodiments have applicability across a wide spectrum of applications.

Detailed Description

A typical optical data transport system will comprise a data source, a data transport layer (framer), a FEC coder, a modulator, a transmitter fiber interface, a fiber connection, a receiver fiber interface, a demodulator, a FEC decoder, a data transport layer de-framer, and a data sink (user). This document will focus primarily on the demodulator and FEC decoder, but solutions presented will impact the design and implementation of other system components.

Digital Demodulator architecture for 40 / 100 Gbps OTN and beyond

Problem 40 / 100 Gbps OTN systems require a digital demodulator to reliably receive the signals at the receiver

The high data rates make the receiver design very complex as very high degree of parallelism is required

Optical channel presents a variety of unique impairments like CD, PMD, PDL and other types of distortions that need to be tracked / corrected digitally

Solution An architecture for a digital receiver that can demodulate the signal in presence of the various optical impairments with very low implementation loss and reasonable implementation complexity that allows for implementation in latest technology ASICs

Technical Keywords OTN, 40 / 100 / 400 / 1000 Gbps, Demodulator, Equalizer, DSP

Novel This is a new demodulator design that can process the signal with all the optical impairments in a highly parallel fashion while keeping reasonable implementation complexity.

Inventors Fan Mo, Bill Thesling, Matt Nimon and Sameep Dave

Digital Demodulator architecture for 40 / 100 Gbps

The Digital Demodulator processes the samples of the analog I and Q components of the two polarization components to recover the transmitted data. At the input side the Demodulator accepts four parallel streams carrying HI (Horizontal I), HQ (Horizontal Q), VI (Vertical I) and VQ (Vertical Q) samples. Each stream will contain multiple samples per clock.

At its output the Demodulator provides demodulated hard-decision data to the HDFEC decoder. The Demodulator may or may not identify the beginning of a FEC frame depending upon the mode of operation. Additionally the Demodulator may receive feedback signals from an internal or external (to the ASIC) HDFEC Decoder regarding the convergence status.

The top level demodulator design is show in Figure 1.

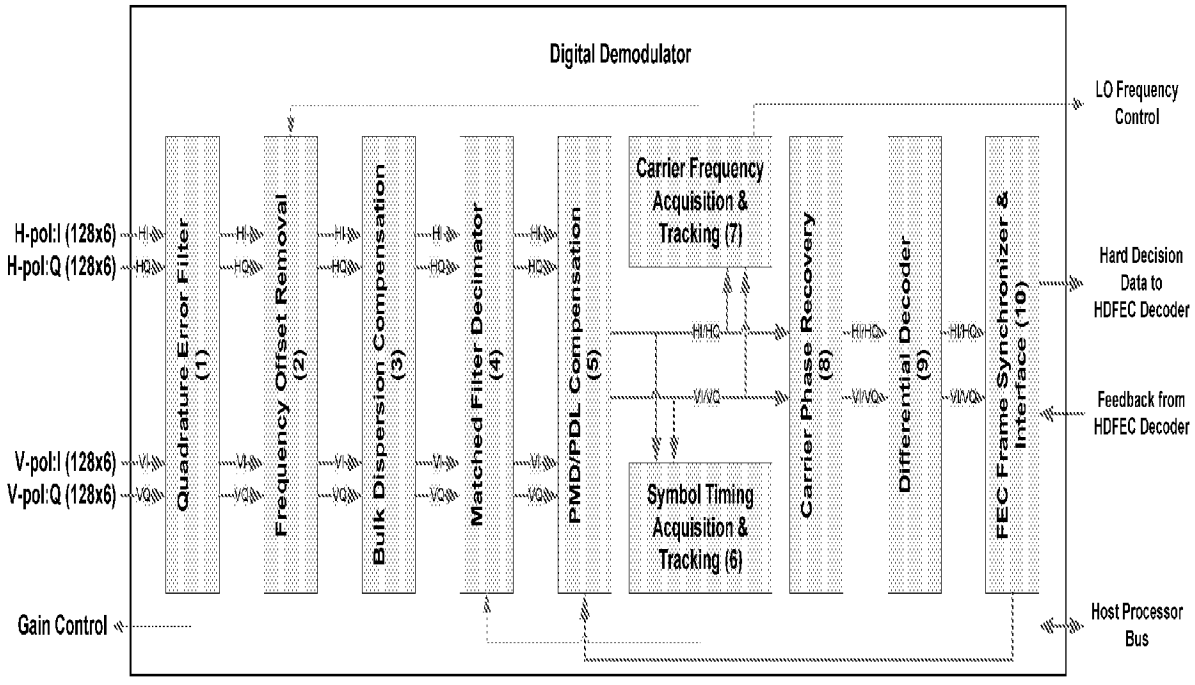


Figure 1: Demodulator Top Level Block Diagram

The Demodulator may have a control and monitor interface bus connected to a host processor allowing for configuration of demodulator parameters (filter coefficients, loop gains, etc.) and extraction of demodulator status.

The following sections detail the functional specification for the major sub-modules within the demodulator design.

Quadrature Error Filters

The Quadrature Error Filter (QEF) module provides a collection of miscellaneous data formatting, error detection and correction functions. Figure 2 shows the top level functional block diagram for the QEF module.

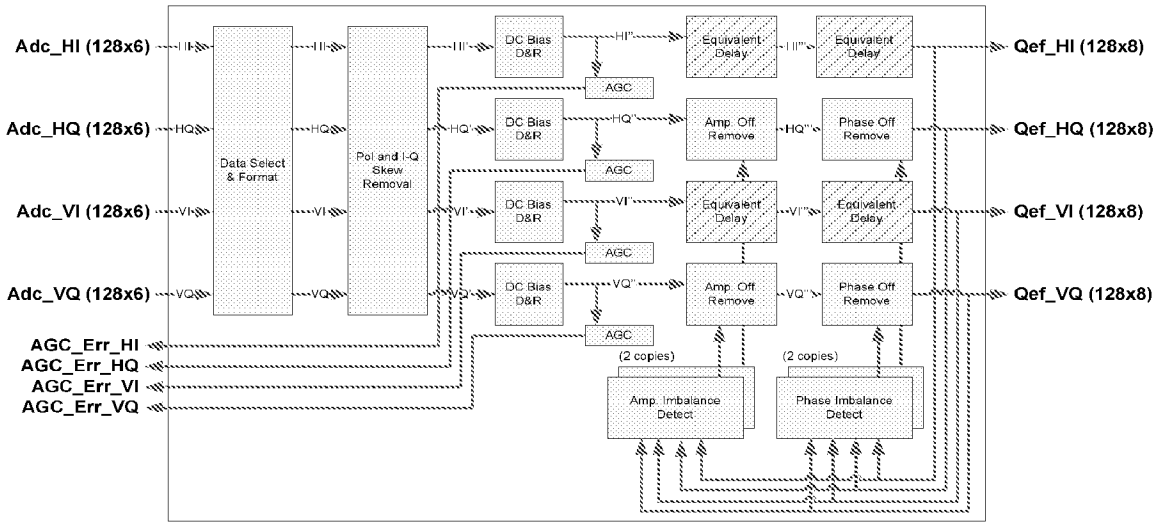


Figure 2: Quadrature Error Filters Top Level

Input data samples are expected to be in binary-offset / offset-binary format coming in from the ADC and it will be converted to the required 2's complement (2C) format for the processing inside the DSP.

The incoming HI, HQ, VI and VQ streams also can be independently swapped and inverted if needed. This allows compensating for any design issues that might translate into an accidental inversion or IQ swap.

Each data stream is processed through a skew correction block to remove polarization skew (between H and V poles) as well as I-Q skew within a pole.

For polarization skew removal a delay element will be used that can delay the poles with respect to each other by a programmable number of integer sample durations. Shift values up to +/- 4 samples will be supported on each pole for a maximum relative offset of +/- 8 samples. This will allow coarse polarization skew removal at calibration time. Any residual sub-sample duration polarization skew at calibration time or any slow time variation in the polarization skew will be tracked out by the PMD equalizer. Please note that this control will be available independently on the I and Q streams within a polarization to help coarse I/Q skew removal.

The QEF module provides for detection and removal of four types of quadrature signal errors: I/Q Skew, DC bias, I/Q amplitude imbalance, and I/Q phase imbalance. All four error detectors can be independently enabled or disabled via the APB processor interface, and the detected error values are output as status values via this same interface.

Frequency Offset Removal

The Frequency Offset Removal (FOR) module will perform a frequency rotation on the data samples coming out of the QEF module. The amount of frequency rotation is controlled by the frequency error input that is sourced by the Carrier Frequency Acquisition and Tracking (CFAT) module. This frequency offset removal function is only intended to remove residual frequency left from the LO laser tuning in the optical domain.

Figure 3 shows the top level block diagram for the frequency offset removal.

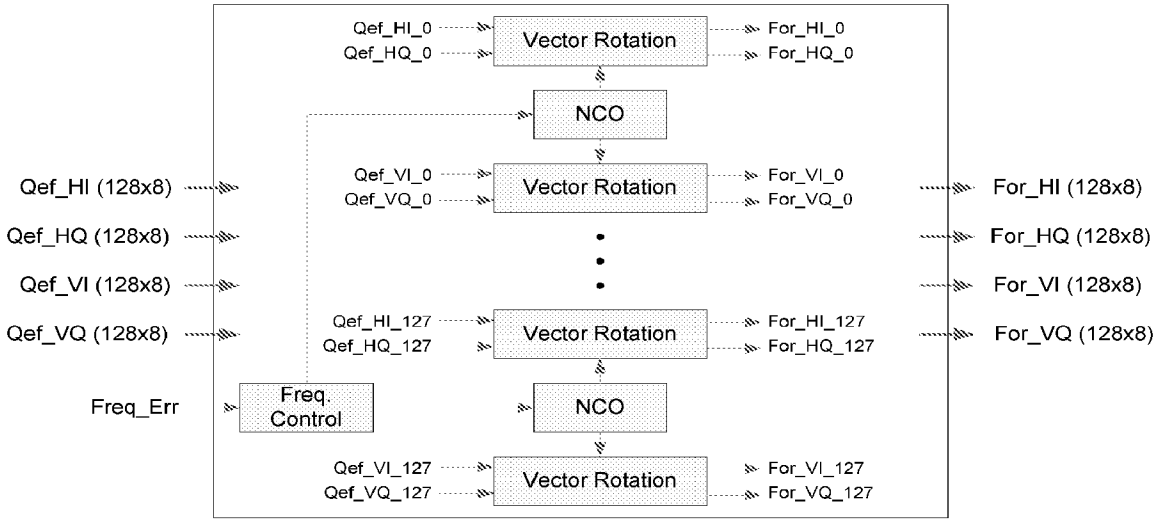


Figure 3: Frequency Offset Removal Top Level

Bulk Dispersion Compensation

The Bulk Dispersion Compensation module removes the bulk Chromatic Dispersion (CD) from the horizontal and vertical polarization channels. The compensation is applied via a filter in the frequency domain. The amount of CD correction is controlled by the CD filter inputs that are derived outside of the demodulator and provided via the host processor control and monitor interface. Figure 4 shows an example top level block diagram for the module.

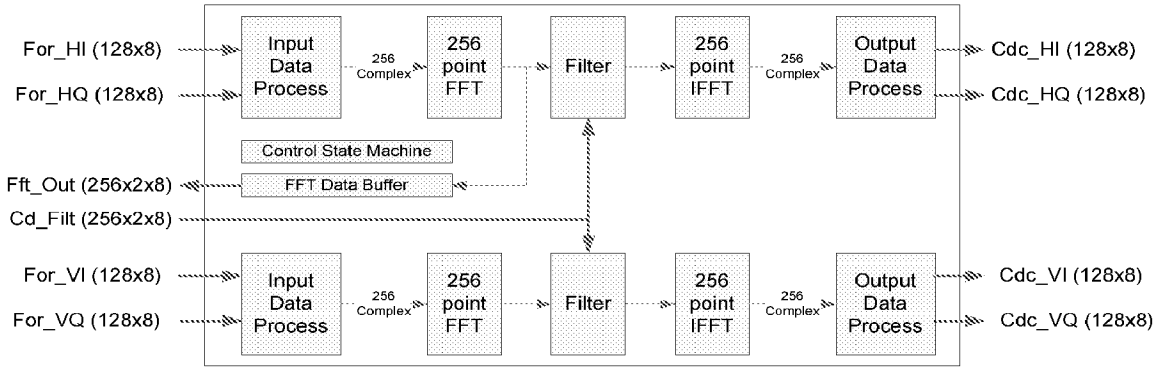


Figure 4: Bulk Dispersion Compensation Top Level

The CD compensation (CDC) for any given sample requires 'input' from a range of data samples before and after the sample.

The Horizontal and Vertical I/Q data pairs are processed through two independent, equivalent processing paths. A single control state machine provides the proper enable and block alignment logic to all other blocks in the module.

The output of the FFT is complex frequency domain data. This data is input to the filter block where a frequency domain filtering operation is performed. The complex FFT outputs are also sent to a data buffer to be read out via the control and monitor block. Note that this is just a snapshot buffer, only a single FFT result is required to be stored at any given time.

The output of the filter block is again complex pairs of CD corrected frequency domain data per clock. The data is input to the 256-point IFFT for conversion back to the time domain. The state machine controls the flow of data through the IFFT.

Matched Filter Decimator

The Matched Filter Decimator (MFD) module implements an interpolation function that provides decimation from the ADC sample rate to 2x the symbol rate. Each of the four

data streams has an independent bank of FIR filters with fixed coefficients. The filter coefficients implement a Raised Cosine (RC) low-pass filter with roll-off of 0.4. The symbol timing error input value fine tunes the decimation rate such that one of the two samples per symbol output is an on-time sample. The sample block assembler takes in the data samples from the filter bank and groups the samples such that valid data output from the MFD block always contains 0 or 128 data samples per clock per stream. Note that valid output data is not available on each clock and the data valid output indicates when valid output data is available. The top level MFD design is shown in Figure 5.

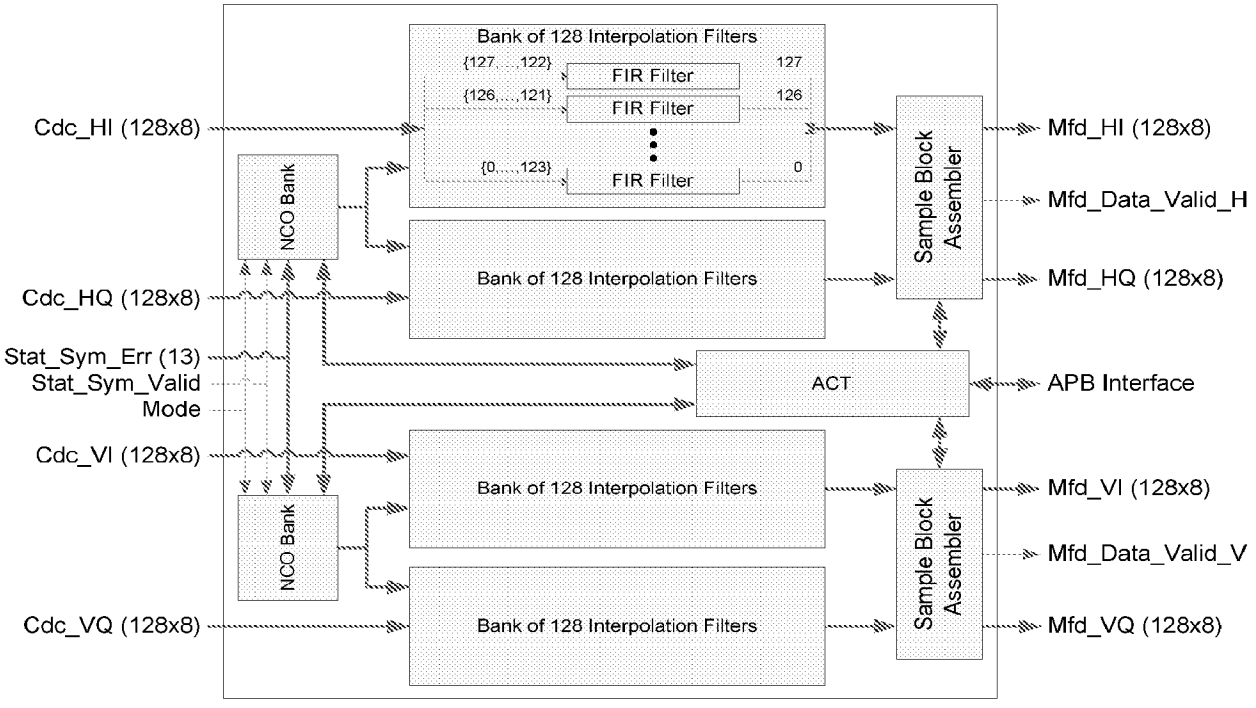


Figure 5: Matched Filter Decimator Top Level

The symbol error is a signed value providing for a maximum symbol timing correction capability of certain % of the baud rate. The symbol timing error is input to the NCO bank where it is added to a nominal NCO step value to produce a corrected NCO step. The nominal NCO step values are pre-computed and fixed for the nominal symbol rates and selected via a configuration register in the ACT block. The corrected NCO step value is also reported as status.

There are four banks of interpolation filters in the module with each banks processing one of the data streams. Each filter bank takes in one data word of sample data and an array of interpolation phases per clock. The filter blocks filter the incoming data through the filter banks with the interpolation phase for each filter driven by the corresponding

interpolation phase value. The filter bank produces 2 samples per symbol out for each data stream.

The decimation rate is controlled by a NCO so the number of output samples produced per clock is not a constant. In order to simplify data processing through the remainder of the Demodulator, data samples are gathered and assembled into blocks of fixed number of samples per stream per clock by the sample block assembler. The assembly function is identical for the I and Q streams in each polarization so one assembly block services two streams.

As the ratio of the output/input samples per clock is not exact, there will be clock cycles where the MFD does not output any data. The Mfd_Data_Valid_x output is asserted only on clocks with valid output data.

The MFD design is optimized for a particular decimation factor. So the ADC sample rate has to be close to $2 + \varepsilon$ times the symbol rate. The ε will be 0.009 for the Polo design.

PMD/PDL Compensation

The PMD/PDL compensation module utilizes adaptive equalization to compensate for the cross polarization interference, IQ channel interference, adjacent symbol interference introduced by PMD and PDL in optical channel and other residual impairments (like residual CD). The adaptive equalizer (EQ) takes in data at 1 or 2 samples/symbol from the MFD and processes the data through a bank of FIR filters with adaptive filter tap coefficients. The top level block diagram for this module is shown in Figure 6.

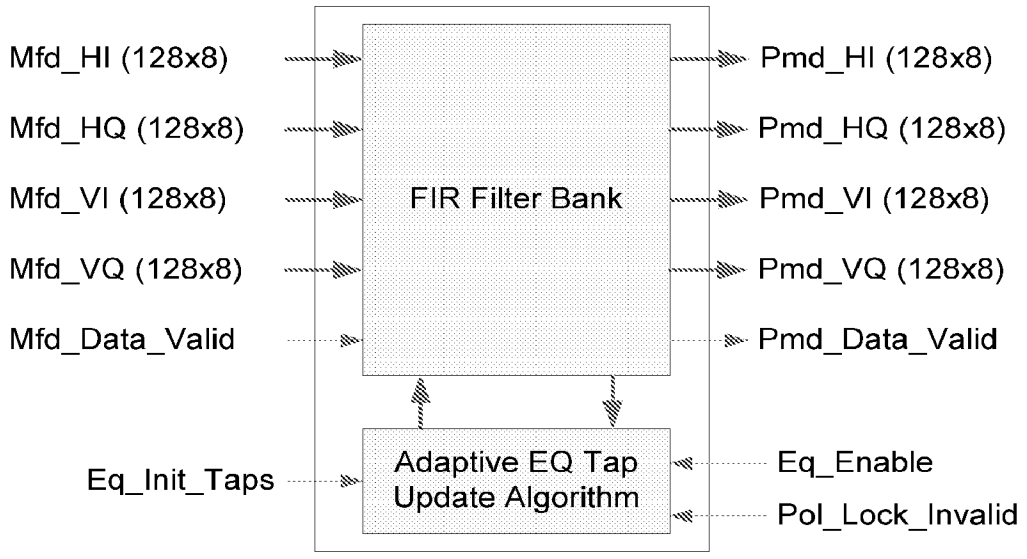


Figure 6: PMD/PDL Compensation Top Level

The FIR filter bank consists of four, 16-tap real or complex filters operating at 1 or 2 taps per symbol. A conceptual view of the filter bank is shown in Figure 7. Each quadrant in Figure 7 is a complex filter.

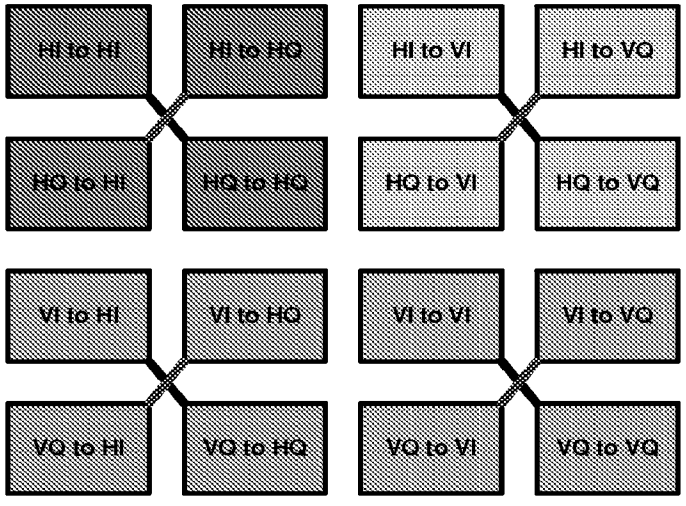


Figure 7: PMD Filter Bank

The filter taps can be initialized through the control and monitor interface. Generally the filters along the diagonal are initialized as all-pass filters with a center tap weight of 1.0

and all other taps set to 0.0. The rest of the filters are initialized with all zero tap weights. The taps are updated by the adaptive EQ tap update algorithm when enabled.

The adaptive EQ tap update algorithm may be a Constant Modulus Algorithm (CMA). This algorithm drives the constellation points on each polarization (at optimal symbol timing) to a circle with the desired radius with minimum radius variation.

The adaptive EQ will converge, with high probability, to a solution that properly decouples the two polarizations. There are however corner cases where the EQ will converge to output the same polarization on both polarization outputs. This error event is detected downstream by the FEC frame synchronizer. When the error is detected, the Pol_Lock_Invalid signal is asserted. The assertion causes the filter taps for the Vertical pole output to be reset.

The module generates all the on-time output samples but generates only half the off-time samples. This helps keep the design size smaller and is sufficient for the symbol timing tracking needs of the following modules.

Symbol Timing Acquisition and Tracking

Symbol Timing Acquisition and Tracking (STAT) may be achieved by means of an early/late symbol radius matching scheme and PI controller. This module also has a symbol timing lock detection mechanism that outputs a symbol lock indicator. There are two sets of gains for the PI controller (wide band for acquisition and narrow band for tracking). When not in timing lock, the wideband gains are used, otherwise, the narrowband gains are used. The top level design is shown in Figure 8.

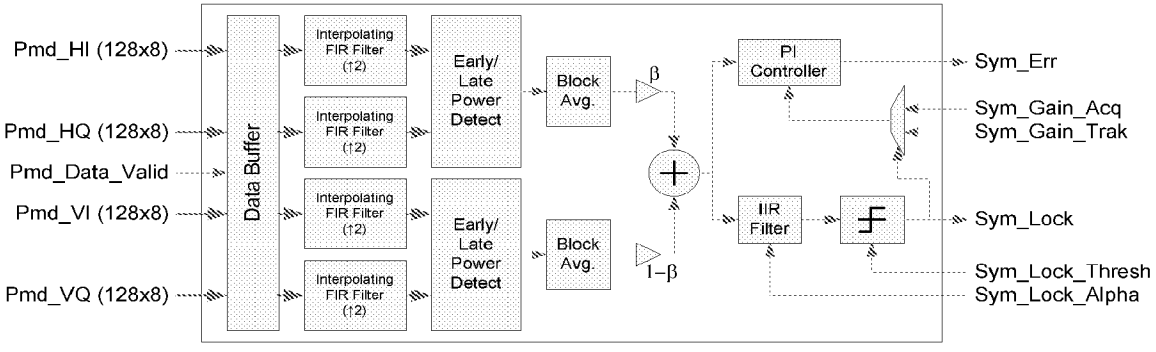


Figure 8: Symbol Timing Acquisition and Tracking Top Level

The incoming I and Q data at 2 samples/symbol represents data samples that are on-time and ½ of a symbol period off from on-time. Each of the incoming data sets (I and Q) is processed through two 12-tap interpolating FIR filters. The FIR filter coefficients are

fixed and have been designed such that one set of filters interpolates the data by ¼ of a symbol period early and the other set by ¼ of a symbol period late.

The early and late I/Q pairs from each polarization are input to a pair of early/late power detection modules. The symbol timing error in each polarization is calculated as the early radius value minus the late radius value. The raw error values are input to a pair of block averaging functions that average the errors.

The average error values from the two polarizations are multiplied by a weighting factor (β) and summed to produce an average symbol timing error for the combined dual-polarization signal. The nominal value for β is 0.50 but it can be programmed in the range {0.0, 1.0}.

The composite average error value is used to update a PI controller once per data block. The PI controller output is the symbol timing error that is fed back to the MFD to adjust the symbol timing. The PI controller gains are selected by the state of the Sym_Lock signal. When not in symbol lock, the wide band acquisition gains are used, otherwise, the narrow band tracking gains are used.

The composite average error value is also used to update an IIR filter. The output of the IIR filter is compared against a user configurable error threshold value. When the filter output drops below the threshold, symbol lock is declared.

Carrier Frequency Acquisition and Tracking

The Carrier Frequency Acquisition and Tracking (CFAT) module is responsible for acquiring as well as tracking carrier frequency. Carrier frequency acquisition is achieved by means of a FFT with appropriate averaging and peak frequency component detection. Carrier frequency tracking is achieved by means of a 2-point DFT with appropriate averaging and variable tracking bandwidth. The frequency error is processed through a PI controller to produce a filtered frequency error. CFAT module also has a carrier frequency lock detection mechanism that outputs a freq_lock indicator. When not in frequency lock, the wide DFT bandwidth is used, otherwise, the narrow DFT bandwidth is used. The freq_lock signal is also used to decide if the FEC frame synchronizer (FFS) module shall forward data to the decoder. The top level design is shown in Figure 9.

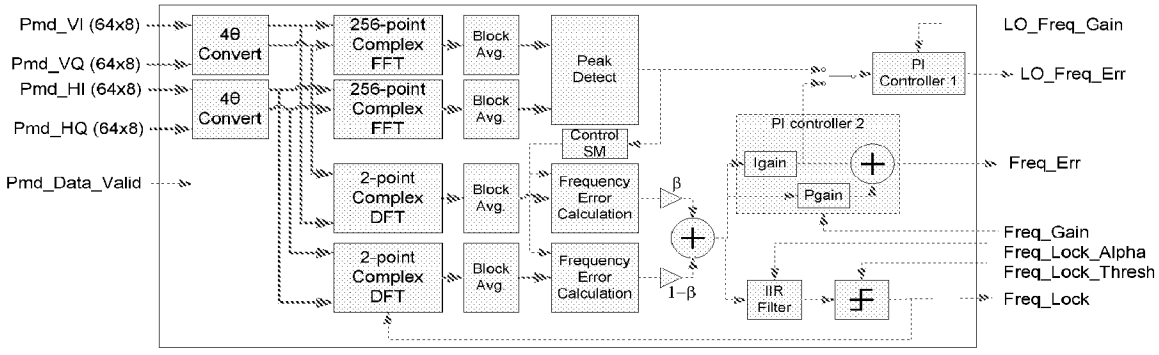


Figure 9: Carrier Frequency Acquisition and Tracking Top Level

The CFAT module operates on the on-time I/Q data samples from both polarizations.

To keep design complexity down, the module does not operate on all data samples, rather on blocks of contiguous symbols once every few clocks to allow processing time between blocks.

The incoming data is processed through a 4θ conversion block to collapse the QPSK modulation down to a tone. The data out of the 4θ conversion block is processed through one of two paths depending on the mode of operation. At start-up the module will be in acquisition mode until the bulk frequency offset measurement is within the tracking bandwidth of the frequency tracking loop. Once that process is complete, the module will operate in tracking mode.

The data output from the 4θ conversion block in this module is output from this module for use in the Carrier Phase Recovery (CPR) module.

Carrier Phase Recovery

Carrier Phase Recovery (CPR) may use a feed-forward algorithm utilizing a Block Phase Estimator (BPE) and a phase rotation function to remove residual frequency and phase errors. CPR module operates on the on-time data samples produced by the PMD compensation module. The top level carrier phase recovery module diagram is shown in Figure 10.

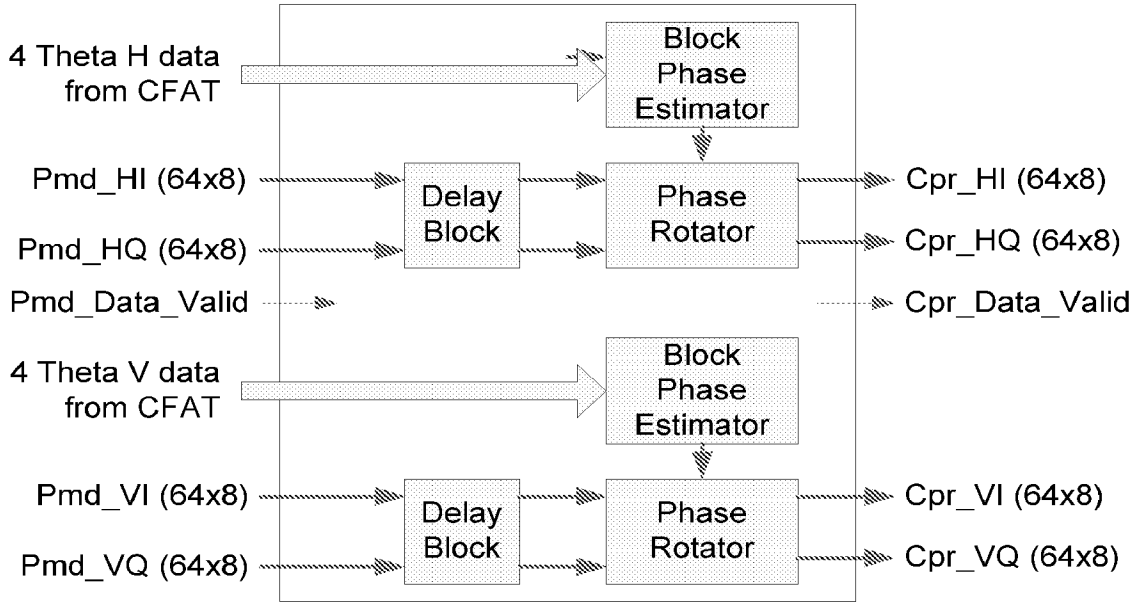


Figure 10: Carrier Phase Recovery Top Level

The on-time data from both polarizations is input and processed through independent, identical processing paths. CPR also needs the I/Q data pairs per polarization to be collapsed to a tone. A similar 4θ conversion occurs in the CFAT module. So the 4θ data is output from CFAT and input to this block thus eliminating the 4θ conversion from this module.

The 4θ data is processed through a BPE to track the phase offsets. The window size of the BPE will be configurable over a small set of fixed values. Within each window, a phase is estimated based on all the 4θ data symbols. The estimation window slides half window size at a time.

The on-time data is also delayed through a delay block to align each symbol in the center of the BPE window.

The delayed data and phase correction value out of the BPE are input to a phase rotator that rotates each symbol by the phase correction value.

Differential Decoder

The Differential Decoder (DDI) module is responsible for accepting symbol streams from the CPR (at 1 sample per symbol) and generating a hard-decision output data stream for the FEC Frame Synchronizer (FFS) module.

In DQPSK mode the incoming data is differentially decoded inside the DDI module and the resulting hard-decision output is sent out to the FFS module.

In QPSK mode the differential decoding is bypassed and just the soft-decision or hard-decision (based on just the sign-bit of the incoming symbol data) is sent out to the FFS module.

The top level block diagram of DDI module is shown in Figure 11.

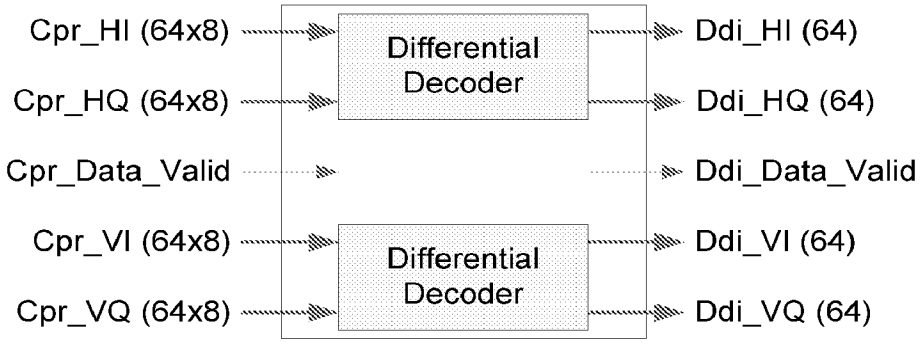


Figure 11: Differential Decoder Top Level

In DQPSK mode DDI uses two consecutive data symbols within the same polarization to figure out the most likely transition which determines the hard-decision information that needs to be sent out to the HDFEC Decoder.

In DQPSK multiple basic pre-coder options may be supported to cover for any transmit and receive implementation mismatches.

Similar flexibility may be provided for QPSK as well where the 2C sign bit of the symbol can be the same as the data bit or the inverse of the data bit.

FEC Frame Synchronizer & FEC Interface

The FEC Frame Synchronizer (FFS) module will help in achieving frame synchronization. The module will consist of three major blocks as shown in Figure 12.

The Data Alignment block may allow several degrees of freedom for skewing, swapping and rotating the channels with respect to each other to help align the channels correctly for the Frame Sync Detection module in the FFS or in an external device be able to decode the channels correctly.

The Frame Sync Detection module in the FFS may implements a hard-decision or soft-decision correlation algorithm with synchronization state machine to search for and synchronize to a known pattern / Unique Word (UW). This module detects and synchronizes to the UWs on both polarizations and helps realign the data stream according to the transmitted order after the UWs have been correctly detected. Note that in mode where UW is not present this module may rely on feedback from an external device that is capable of providing feedback signals to help the Data Alignment block tweak the alignment between the channels till correct synchronization is achieved.

The Clock Transfer module may be responsible for taking the parallel data bus at the internal core clock to a different format bus at a clock speed suitable for the Decoder / Deframer following the DSP.

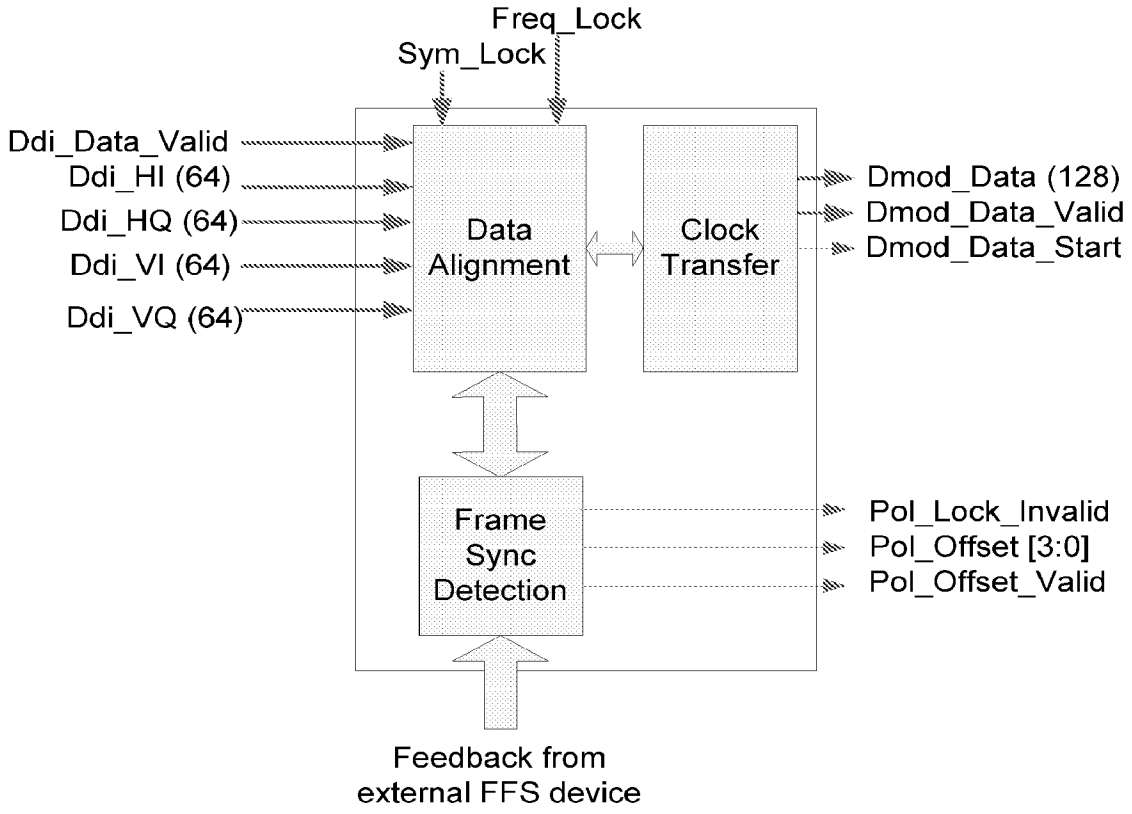


Figure 12: FEC Frame Synchronizer and FEC Interface Top Level

Hard or soft correlation may be used to correlate the incoming complex samples in each polarization with the expected complex UW pattern. The correlation results are compared to a programmable threshold to decide if UW is detected. In DQPSK mode there is no need to solve the IQ phase ambiguity within each polarization. Only in-phase correlation (I to I, Q to Q) is required. And the correlation peak will always be positive.

In QPSK mode this module will resolve the phase ambiguity at every UW.

Soft-input generation for soft-decision FEC decoding of a differentially encoded signal

Problem Currently in 40 / 100 Gbps OTN (Optical Transport Network) systems hard-decision FEC (Forward Error Correction) schemes are being used.

Also because of high phase noise differential encoding is being applied.

Soft-decision FEC (SDFEC) provides higher performance gains if a good quality soft-input can be generated for the Decoder in presence of differential encoding.

Solution Algorithm for soft-input / LLR generation that preserves the BER-in / BER-out relationship for the SDFEC and is suitable for high speed implementation Simplifications to the algorithm for high-speed implementation

Technical Keywords Soft-decision decoding, differential encoding / decoding, DQPSK, SDFEC

Novel This is a new technique. In 40 / 100 Gbps OTN use of SDFEC is not prevalent. Just generating a soft-input / LLR that preserves the SDFEC performance is a innovation. Applying this at 40 / 100 Gbps with low implementation complexity is another innovation.

Inventors Fan Mo and Sameep Dave

Differential Encoding & Decoding Algorithm

Differential Encoding

The Differential encoding is applied with QPSK modulation separately in horizontal and vertical polarizations. Figure 1 shows the differential encoding method. The red constellation dots, labeled as (DI,DQ), represent the output QPSK symbols from the differential decoder. The transition between the constellation symbols are decided by the input symbols, labeled as (CI, CQ), to the differential encoder.

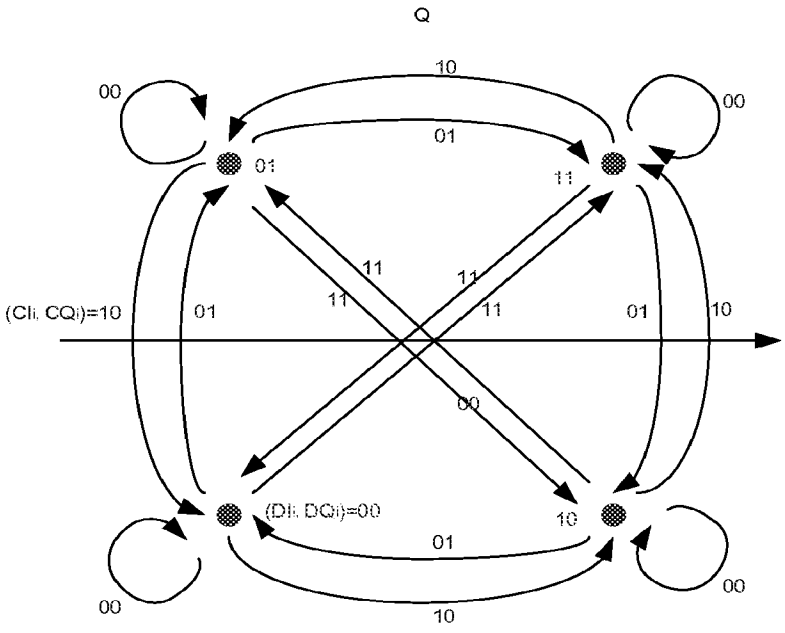


Fig. 1 Differential encoding method

The differential encoder follows the following rules:

Initialization: assume the previous transmitted symbol pattern is 00 so (DI_{-1}, DQ_{-1}) = (-0.707, -0.707)

If the input symbol (CI_0,CQ_0) to the differential decoder at time 0 is

00: no rotation is applied, (DI_0,DQ_0) = (-0.707, -0.707).
01: 90-degree clockwise rotation is applied, (DI_0,DQ_0) = (-0.707, 0.707).
10: 90-degree counter-clockwise rotation is applied, (DI_0,DQ_0) = (0.707, -0.707).
11: 180-degree rotation is applied, (DI_0,DQ_0) = (0.707, 0.707).

Let's assume the pattern for (CI_0,CQ_0) is 10 so (DI_0,DQ_0) = (0.707, -0.707). If the input symbol (CI_1,CQ_1) to the differential decoder is

00: no rotation is applied, (DI_1,DQ_1) = (0.707, -0.707).
01: 90-degree clockwise rotation is applied, (DI_1,DQ_1) = (-0.707, -0.707).
10: 90-degree counter-clockwise rotation is applied, (DI_1,DQ_1) = (0.707, 0.707).
11: 180-degree rotation is applied, (DI_1,DQ_1) = (-0.707, 0.707).

And encoding will be performed continuously following this method.

Differential Decoding

The Differential decoding for is performed in each polarization after coherent QPSK detection. The hard decisions of (CI_i, CQ_i) are made based on judging the most likely transition between each pair of received symbols, (DI_{i-1}, DQi_{-1}) and (DI_i, DQ_i) (noise corrupted at the receiver). The Table 1 below summarizes all the hard decision cases.

Table 1 Hard decision decoding

Case index	(DI_{i-1}, DQi_{-1})	(DI_i, DQ_i)	(CI_i, CQ_i)
0	00	00	00
1	00	01	01
2	00	10	10
3	00	11	11
4	01	00	01
5	01	01	11
6	01	10	00
7	01	11	10
8	10	00	10
9	10	01	00
10	10	10	11
11	10	11	01
12	11	00	11
13	11	01	10
14	11	10	01
15	11	11	00

To achieve the best performance from the down stream SDFEC decoder, we have to also generate the soft input information that represents the reliability of each bit. The ideal method to generate the soft input is to generate maximum-likelihood ratio (LLR) as the input to the decoder. The general Equation for LLR is:

$$LLR_{b_{i_1}} = \frac{\sum P(b_i = 1)}{\sum P(b_i = 0)} \quad (1)$$

For instance for the bit CI_i, cases 2 3, 5,7, 8, 10, 12 and 13 in Table 1 are corresponding to a hard decision of $CI_i = 1$ and the rest of the cases are corresponding to hard decision of $CI_i = 0$. So the

$$LLR_{CI_i} = \frac{P(00,10) + P(00,11) + P(01,01) + P(01,11) + P(10,00) + P(10,10) + P(11,00) + P(11,01)}{P(00,00) + P(00,01) + P(01,00) + P(01,10) + P)(10,01) + P(10,11) + P(11,10) + P(11,11)} \quad (2)$$

Here P((DI_{i-1}, DQi_{-1}), (DI_i, DQi)) represent the probability of transition from (DI_{i-1}, DQ_{i-1}) to (DI_i, DQ_i). A total of 16 terms are involved here in the computation so the computational complexity is extremely high. One way to avoid all the real time

computations is to is to use pre computed look-up tables (LUTs). However for high speed designs we have large number of parallel path which will make the LUTs too large to implement. Therefore a simplified algorithm is defined here. Simulations have proved that this simplified method provides insignificant performance degradation compared to using optimal LLRs.

The key for the simplified algorithm is to identify the dominating terms in computing the LLR. The following set of figures in Fig. 2 helps to identify the terms. The blue dots represent (DI_{i-1}, DQ_{i-1}) and the red dots represent (DI_i, DQ_i). To help identify the cases we assume (DI_{i-1}, DQ_{i-1}) is always in the third quadrant, and (DI_i, DQ_i) is moving from 1st quadrant to 4th quadrant in each row. In row 1, DI_{i-1} has the smallest magnitude for cases A to D. In row 2, DQ_{i-1} has the smallest magnitude for cases E to H. In row three, DQ_i has the smallest magnitude in the first quadrant for case I and the red dot is rotated by 90, 180 and 270 degrees for case J to L. In row 4, DI_i has the smallest magnitude in the first quadrant for case I and the red dot is rotated by 90, 180 and 270 degrees for case N to P. All these 16 cases combined cover all relative magnitude possibilities with (DI_{i-1}, DQ_{i-1}) in the 3rd quadrant. By examine the cases we find out for each case what is the most likely transition (represented by (CI_i, CQ_i)) and what is the second likely transition. These two transitions are then used to help us to decide how the LLR information for (CI_i, CQ_i) shall be collected.

For example, for case A, the most likely transition is (CI_i, CQ_i) =11 (transition from (DI_{i-1}, DQi_{-1})=00 to (DI_i, DQi) = 11). Since DI_{i-1} has the smallest magnitude among all, the second most likely transition is (CI_i, CQ_i) =10 (from (DI_{i-1}, DQ_{i-1}) =10 to (DI_i, DQi) = 11 with DI_{i-1} flipped sign). The reliabilities of (CI_i, CQ_i) are decided by both (DI_{i-1}, DQ_{i-1}) and (DI_i, DQ_i). G operation, which computes the joint reliability of two reliability values, is used to calculate the reliability of CI_i and CQ_i. In this case the G operation between (DI_{i-1}, DI_i) should be assigned to CQ_i as the reliability information. This is intuitive since that the flip of CQ_i is most likely event. On the other hand, the G operation between (DQ_{i-1}, DQ_i) should be assigned to CI_i as the reliability information.

In another example of case B, the most likely transition is (CI_i, CQ_i) =01 (transition from (DI_{i-1}, DQi_{-1})=00 to (DI_i, DQi) = 01). Since DI_{i-1} has the smallest magnitude among all, the second most likely transition is (CI_i, CQ_i) =11 (from (DI_{i-1}, DQ_{i-1}) =10 to (DI_i, DQi) = 01 with DI_{i-1} flipped sign). In this case the G operation between (DI_{i-1}, DI_i) should be assigned to CI_i as the reliability information since the flip of CI_i is most likely event. On the other hand, the G operation between (DQ_{i-1}, DQ_i) should be assigned to CQ_i as the reliability information.

By analyzing all 16 cases, we found that 4 of the cases: A, C, E and G shall have the G operation between (DI_{i-1}, DI_i) assigned to CQ_i and the G operation between (DQ_{i-1}, DQ_i) assigned to CI_i while in all other cases, the G operation between (DI_{i-1}, DI_i) should be assigned to CI_i and the G operation between (DQ_{i-1}, DQ_i) should be assigned to CQ_i, we summarized these cases in Table 2.

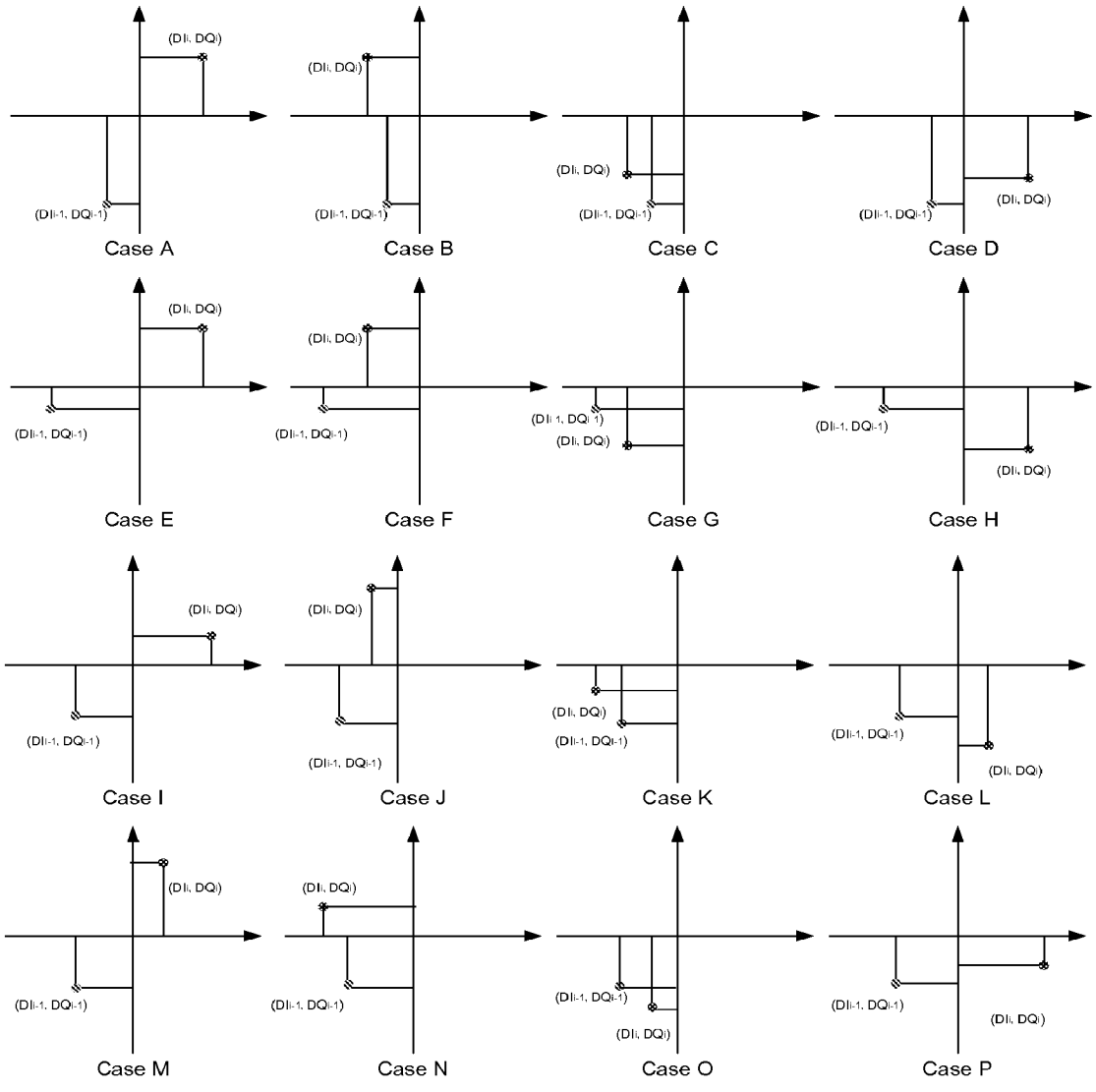


Figure 2: Diff decoding case analysis

Table 2 Reliability assignment for Diff decoder

Case index	Most likely transition (DI_i, DQ_i)	Second most likely transition (DI_i, DQ_i)	Reliability assignment CI_i	Reliability assignment CQ_i
A	11	10	$G(DQ_{i-1}, DQ_i)$	$G(DI_{i-1}, DI_i)$
B	01	11	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
C	00	01	$G(DQ_{i-1}, DQ_i)$	$G(DI_{i-1}, DI_i)$
D	10	00	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
E	11	01	$G(DQ_{i-1}, DQ_i)$	$G(DI_{i-1}, DI_i)$

F	01	00	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
G	00	10	$G(DQ_{i-1}, DQ_i)$	$G(DI_{i-1}, DI_i)$
H	10	11	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
I	10	11	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
J	01	11	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
K	00	01	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
L	10	00	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
M	11	01	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
N	01	00	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
O	00	10	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
P	10	11	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$

The above analysis covers only the cases when (DI_{i-1}, DQ_{i-1}) is in the third quadrant. All other cases with (DI_{i-1}, DQ_{i-1}) in other quadrant are also analyzed.

CDSLLDFT method for tuning very large frequency offsets in 40 / 100 Gbps OTN

Problem Potential for very large starting frequency offset in 40 / 100 Gbps OTN (Optical Transport Network) systems.

Generating error signals to help tune the LO to bring the signal to baseband.

Solution Algorithm for detecting the presence of large frequency offset and providing correction direction / value for appropriate tuning

Reusing frequency bins from the frequency domain CD compensation circuitry
Technical Keywords LO Tuning, LASER tuning, frequency offset

Novel This is a new technique. In 40 / 100 Gbps OTN systems the Rx LO can be way off (several GHz). The invention is a low implementation complexity solution to help achieve lock.

Inventors Matt Nimon, Fan Mo, Bill Thesling and Sameep Dave

Coarse Frequency Estimation

The demodulator may need to operate with large frequency offsets (larger than the symbol rate). The CFAT module is capable of acquiring the input signal in presence of frequency offsets up to ±12.5% of the symbol rate. The FFT capability of the CDC module is used to provide a coarse indication of frequency offset to help bring down the frequency uncertainty to within the ±12.5% range. This is accomplished as described below.

Four samples are taken at the output of the FFT, the FFT bins selected will be programmable through the ACT interface. These 4 samples are referred to in what follows as samples A, B, C, and D, respectively. These 4 samples will be taken and processed every frame (clock).

The magnitude (radius) of each of these 4 samples is computed using the CORDIC common module. Those 4 computed magnitudes are called |A|, |B|, |C|, and |D|, and they are each represented by 9 bits. Each of these magnitudes are filtered via a first order IIR filter transfer function H(z), with programmable alpha, as shown below.

$$H(z) = \frac{alpha}{1-(1-alpha)z^{-1}}$$

The filtered quantities f(|A|), f(|B|), f(|C|), and f(|D|) are then combined algebraically to form the frequency metric as: f(|A|) + f(|B|) - f(|C|) - f(|D|) represented by 11 bits.

The output is brought to the ACT interface where it can be read as a read only status register.

In addition, the filtered quantities are input to a decision block that determines if the frequency offset is high or low. In this block the value: max(f(|A|), f(|B|), f(|C|), f(|D|)) – {(f(|A|)+ f(|B|) + f(|C|) + fl(D|))/4} is computed. If this value less than an programmable input threshold then one of two interrupts (irq_coarse_freq_offset_hi or irq_coarse_freq_offset_lo) is triggered based on the sign of f(|A|) + f(|B|) - f(|C|) - f(|D|) .

The following block diagram provides the low level details:

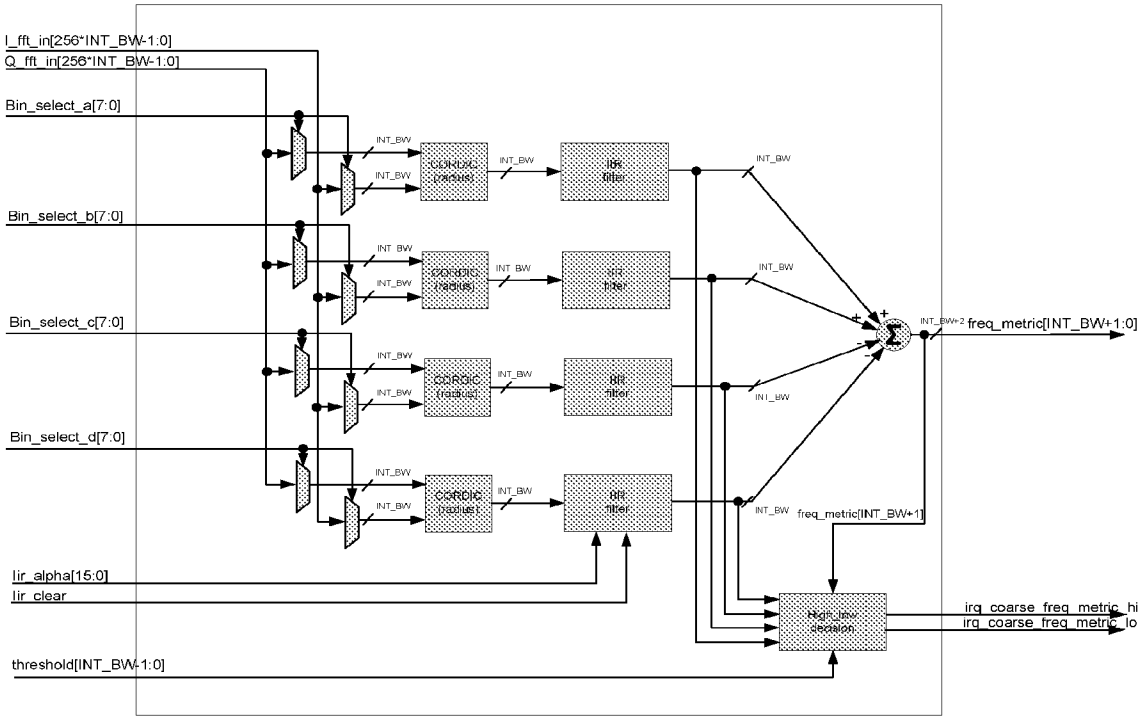


Figure 1. Coarse frequency estimation metric block diagram

Adaptive PMD Equalizer and Implementation

Problem In 40 / 100 Gbps OTN (Optical Transport Network) systems dual-pole transmission is used.

Optical fiber imperfections result in signals interfering across poles. This phenomenon is termed as PMD (polarization mode dispersion)

This interference can change over time and needs to be tracked out

PMD if note recovered can greatly affect the receiver performance

Solution Algorithm for tracking PMD using a CMA based Equalizer that works across both poles
Dual modes for error signal generation
Real and complex incarnations of the Equalizer
Equalizer partitioning for ASIC implementation

Technical Keywords PMD, Equalizer, PM-QPSK, PM-DQPSK, 40 / 100 Gbps, OTN

Novel This is a new approach for tackling PMD. One of the biggest complexity contributors to the receiver design. We have looked at a variety of approaches to make it more manageable for ASIC implementation.

Inventors Fan Mo, Sameep Dave, and Lawrence Esker

Adaptive PMD Equalizer and Implementation

The PMD/PDL compensation module utilizes adaptive equalization / equalizer (EQ) to compensate for PMD (a type of cross polarization interference), PDL (varying received signal strength between poles), and miscellaneous residual impairments that translate into interference / undesired interaction between samples of the same channel / stream / tributary (I or Q samples in a pole. So in DPQPSK transmission we have 2 channels per pole and 4 channels total), or samples of the other channel in the same pole, or samples of other channels across both poles.

The PMD/PDL compensation module takes in data at 2 samples/symbol from the MFD (Matched Filter Decimator) module and processes the data through a bank of FIR filters with adaptive filter taps / coefficients. The filtered output is sent to the STAT (Symbol Timing Acquisition and Tracking), CFAT (Carrier Frequency Acquisition and Tracking) and CPR (Carrier Phase Recovery) modules. STAT gets 2 samples (on-time and off-time) per symbol for half of the symbols (32 contiguous on-time and off-time symbols per valid clock) while CFAT and CPR get 1 sample (on-time) per symbol for all the symbols (64 contiguous on-time symbols per valid clock). The top level block diagram for this module is shown in Figure 6.

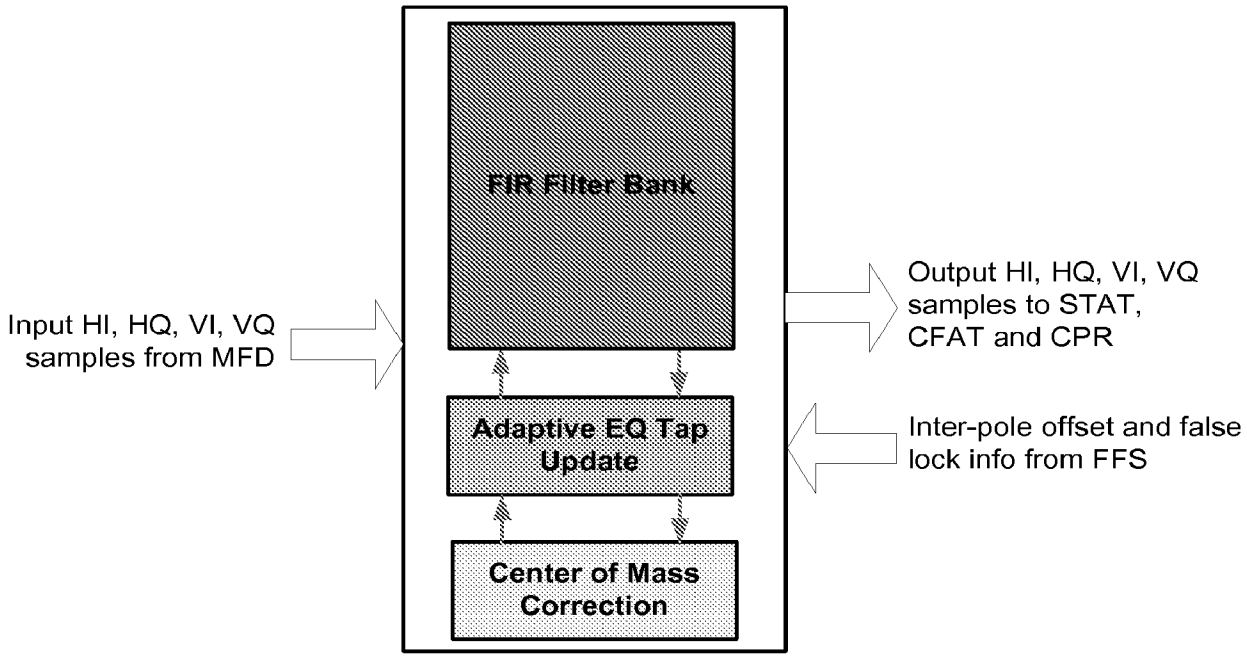


Figure 13: PMD/PDL Compensation module Top Level

The FIR filter bank shown in Figure 6 consists of sixteen, 16-tap real FIR filters operating at 2 taps per symbol. A conceptual view of the filter bank is shown in Figure 7.

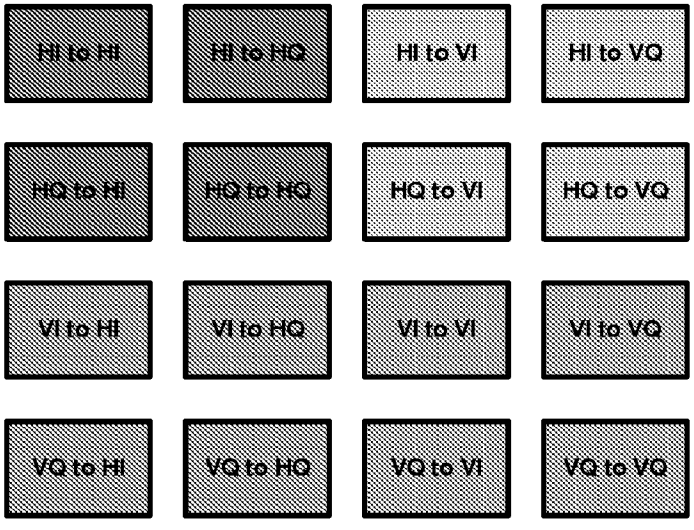


Figure 14: PMD/PDL Compensation module Filter Bank

Each box in Figure 7 represents a 16-tap FIR Filter. The boxes are marked to indicate that they are responsible to cover the impact of which input channel to which output channel. For example the HI to VQ box means the filter is calculating the impact of HI (Horizontal-pole In-phase signal) on to VQ (Vertical-pole Quadrature-phase signal). So every row in the Figure 7 represents the impact of a certain input channel on every output channel. And every column represents the impact of all input channels onto a particular output channel. (1) shows the math behind the HI output generated by the first column in Figure 7 :

$$Out_{HI,n} = \sum_{i=-7}^{8} \left(In_{HI,n+i} \times T_{HI2HI,i} + In_{HQ,n+i} \times T_{HQ2HI,i} + In_{VI,n+i} \times T_{VI2HI,i} + In_{VQ,n+i} \times T_{VQ2HI,i} \right) \quad (1)$$

Where

n is the sample index (lower number is earlier in time),

i is index variable,

Out is the output sample where the first subscript shows the output channel and second subscript is the sample index,

In is the input sample where the first subscript shows the input channel and second subscript is the sample index,

and T is the set of filter taps where the first subscript shows which of the 16 filters (have use *2* notation instead of * to *) and the second subscript is the tap index assuming a 16-tap filter where index 0 is the center tap. Please note that for C or RTL indexing the taps may be numbered from 0 to 15 with 7 being the center tap. As longs as the indexing is consistent in terms of functionality we will be in good shape.

Midway through the system design and simulations it was decided that for some applications of PMD/PDL compensation module we will use complex FIR filters. What this translates into is that each quadrant (same color boxes) in Figure 7 is a complex filter instead of the four real filters shown. The complex filter decision took one degree of freedom away and so now within a quadrant the filters that are diagonally across to each other have the same taps or taps that are opposite in sign. Figure 15 shows the interdependence of the taps in case of complex filtering. The taps for filters connected by the black line (negative slope diagonal) are the same while the taps for filters connected by the red line (positive slope diagonal) are opposite in sign.

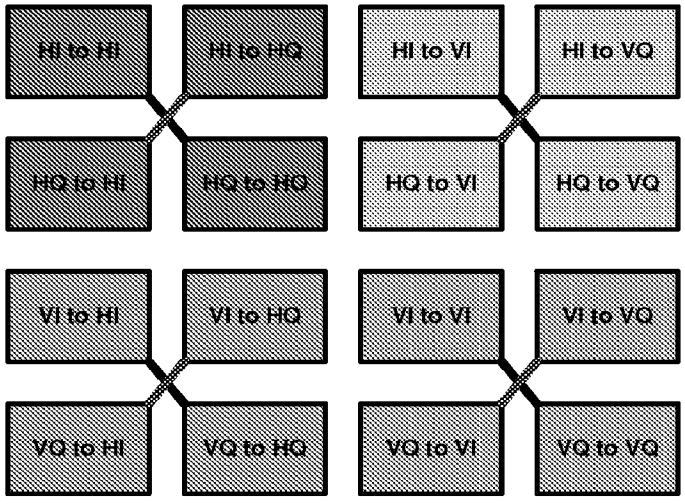


Figure 15: PMD/PDL Compensation module complex FIR filter bank

For the filter tap updates on POLO CMA (Constant Modulus Algorithm) is used. CMA drives the on-time (at optimal symbol timing) constellation points on each polarization to a circle with a desired radius with minimum radius variation. The filter taps are usually initialized as an all-pass filter with only the center taps $T_{HI2HI,0}$, $T_{HQ2HQ,0}$, $T_{VI2VI,0}$ and $T_{VQ2VQ,0}$ initialized to unity while rest of the taps are all zeroes. And using only on-time output samples the filter taps are updated using an error signal as shown in (2) or optionally a simpler mechanism shown in (3).

$$T_{HI2HI,i,n} = T_{HI2HI,i,n-1} + (\beta - (Out_{HI,n}^2 + Out_{HQ,n}^2)) \times Out_{HI,n} \times In_{HI,n+i} \times \mu) \quad (2)$$

$$T_{HI2HI,i,n} = T_{HI2HI,i,n-1} + sign(\beta - (Out_{HI,n}^2 + Out_{HQ,n}^2)) \times Out_{HI,n} \times In_{HI,n+i} \times \mu) \quad (3)$$

Where

Out^2 is the squared on-time output sample where the first subscript shows the output channel and second subscript is the sample index,

β is desired threshold (squared radius) which CMA is driving towards,

μ is a gain factor that affects the speed and stability of CMA's convergence,

sign(.) is just calculating the sign of the operand,

and rest of the variables have the same meaning as in (1).

The adaptive EQ receives a few feedback signals from the FFS (FEC Frame Synchronizer) module. In certain fiber channel conditions the filter taps can converge such that the outputs on both poles is the same (both are locked to H or both are locked to V). In such cases the FFS indicates that the polarization lock is invalid and EQ will reinitialize the taps (to their default value as configured via the APB interface) that generate the Vertical pole (filters in the right half of Figure 15). This re-initialization

should result in the EQ converging on different poles. This process can be performed recursively till the desired convergence is achieved.

Also at initial acquisition stage if the FFS detects a timing offset between the two poles it will convey that offset value to the EQ so that the filter taps can be re-initialized or shifted to compensate for the offset. This offset is performed in a balanced fashion between the filter taps generating the outputs for the two poles to make sure sufficient taps are available towards the edge of the filter. If such compensation is not performed the EQ might converge such that during normal operation the higher weight taps (on one of the poles at any time) get skewed towards the edge of the filter essentially turning the EQ into a filter with small number of useful (relatively bigger value) taps.

The EQ is also a part of the symbol timing loop along with the STAT module. The EQ can interact with the symbol timing loop in such a fashion that at times the EQ filter taps on both poles can start drifting towards the edge of the filter, again turning the EQ into a filter with small number of useful taps. CoM evaluation and correction will be performed in the PMD / PDL compensation module to make sure that if the useful EQ taps have shifted by a symbol they are moved back towards the center of the filter. To figure out if the taps have moved the CoM will be calculated as the difference between the combined tap energies of the filter taps index -7 to -1 and filter taps index 1 to 7. If the magnitude of this difference is greater than a programmable threshold the taps are instantaneously adjusted towards the center. Please note that adjustment of taps will result in addition or deletion of a symbol and needs to be accompanied by the deletion or addition (respectively) of a symbol in the data going out (to CPR and CFAT).

A combination of the FIR filter bank, the CMA update algorithm and tap / output adjustments based on CoM and feedback from FFS will lead to a stable and powerful PMD / PDL compensation design.

I/Q Skew compensation / tracking in 40 / 100 Gbps OTN

Problem Small I versus Q timing skew / offset can cause huge performance degradation in 40 / 100 Gbps OTN (Optical Transport Network) systems.

Evaluating the I versus Q skew in the presence of various optical impairments is very challenging.

This skew can vary over time / temperature and needs to be tracked.

Solution Algorithm for generating a reliable error signal for measuring I versus Q skew in the presence of miscellaneous high speed board design related issues as well as optical impairments like CD, PMD,

Algorithm for removing I versus Q skew at calibration

Low complexity algorithm for tracking and correcting changes in I versus Q skew over time

Technical Keywords I/Q Skew, I versus Q skew, Sampling time offset

Novel This is a new technique. In 40 / 100 Gbps OTN systems very small (several ps) skew between I and Q channels of a QPSK signal is a big fraction of the symbol duration and very detrimental to performance. Generating an error signal that provided basis for correction in presence of all the impairments was very challenging. The techniques to use this error signal at calibration time as well as run-time are also new innovations.

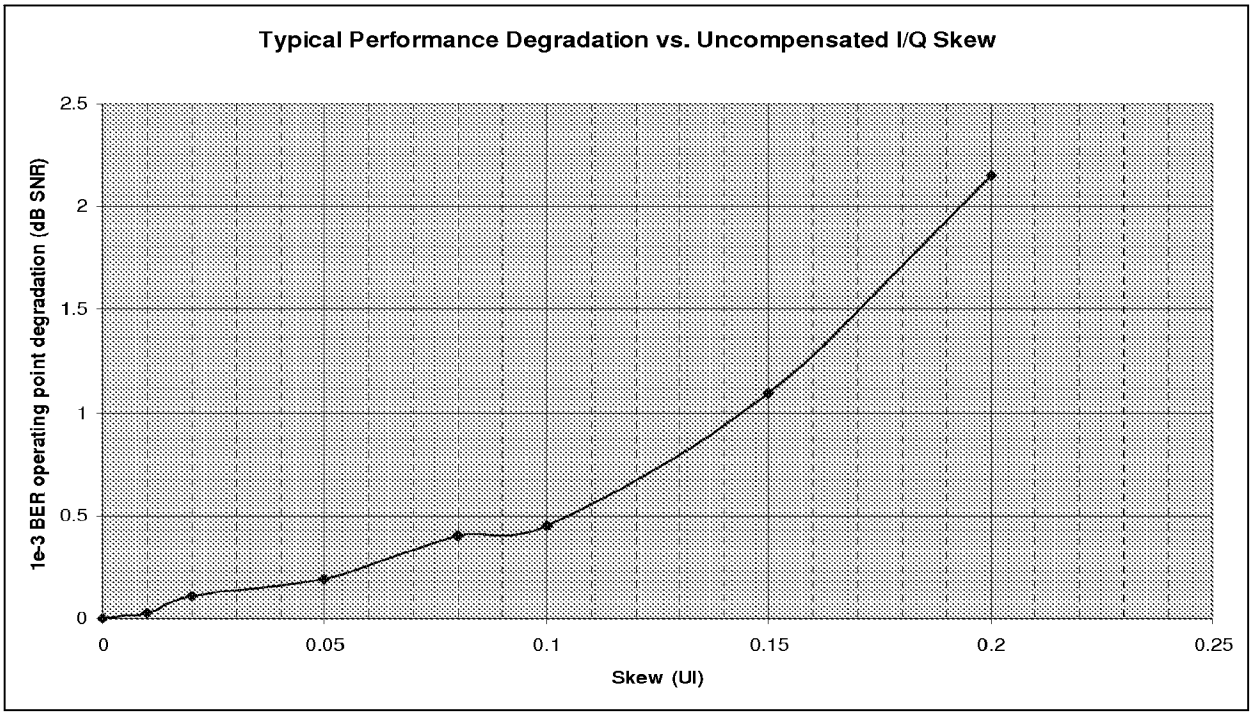
Inventors Yuri Zelensky and Fan Mo

I/Q Skew compensation / tracking in 40 / 100 Gbps OTN

Most current designs for a digital demodulator try to compensate for three types of quadrature demodulator imperfections – DC offset, Amplitude Imbalance and Phase Imbalance. As data rates increase an additional impairment can become an issue – a propagation skew between the I and the Q channel. This impairment behaves differently from the other three and requires a different approach. One way that this was handled in the past was to have an initial skew compensation calibration in the digital domain to calibrate out the imperfections in a given receiver. However, as data rates are increasing, the thermal drift over time can become significant enough in order to merit a real-time adaptive skew-compensation circuit.

If skew is left uncompensated, it can lead to severe degradation in demodulator performance. Below is an example set of simulated performance for a 40Gbps optical demodulator with a comprehensive set of other channel impairments, recording an expected post-demodulator 1e-3 BER SNR operating point in the presence of various

amounts of uncompensated I/Q skew. I/Q skew is measured as a fraction of UI (Unit Interval) or symbol interval, where a symbol interval is two ADC samples:



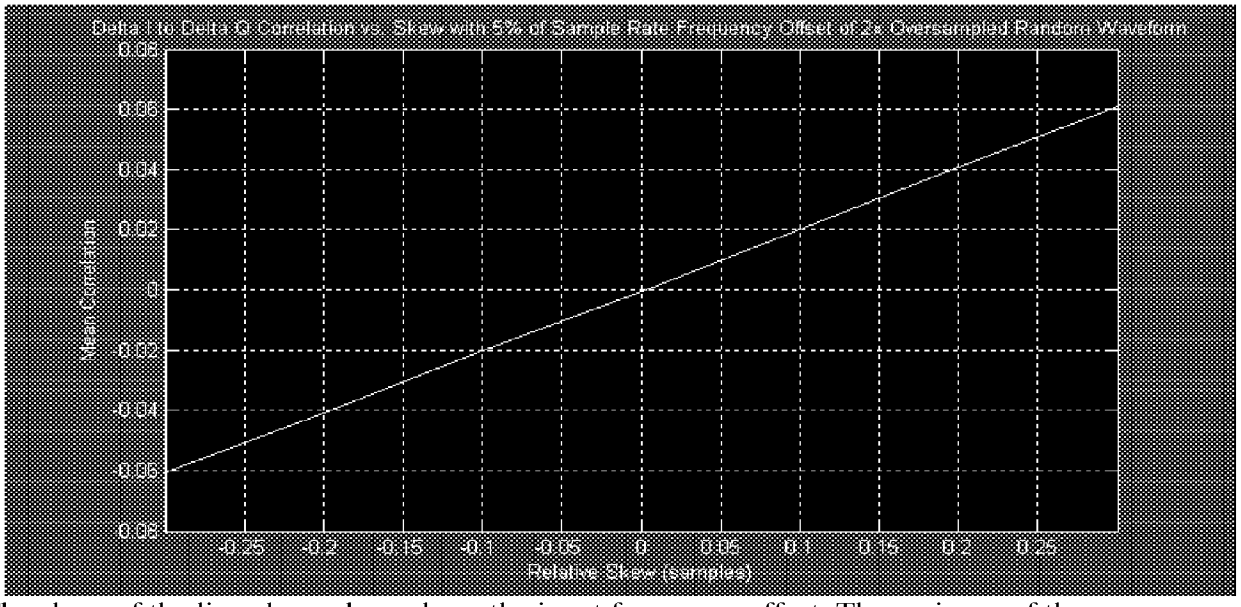
From above, in this particular case a 2% UI skew causes about 0.1dB performance degradation, while a 20% UI skew causes over 2dB of degradation. The total amount of degradation will depend on the relative operating point that is being examined – in this case it is around 11 dB SNR.

Analysis

From a practical perspective, our goal is to find some metric of the received ADC samples that indicates if there is a significant amount of timing skew between the two channels. Because we know that skew causes performance and EsNo degradation, the most straight forward way is to demodulate signal with different amounts of up-front skew and pick the skew amount that maximizes receive EsNo. This is a practical approach during initial calibration, but if skew adjustment is required during normal operation this would require either 2 fully-parallel demodulators or a constant performance degradation as different amounts of skew are tried – first case being impractical from demodulator size perspective and second from performance perspective. If the input signal is relatively well behaved (not too many channel impairments) it is possible to perform a signal quality estimation early in the demodulator chain and not need two fully parallel paths – just one main path and a secondary path that tries alternative skew amounts and processes data to a certain extent in order to extract a meaningful quality estimate. Unfortunately, in a high-speed optical channel, impairments such as Chromatic Dispersion, Polarization Mode Distortion and significant carrier

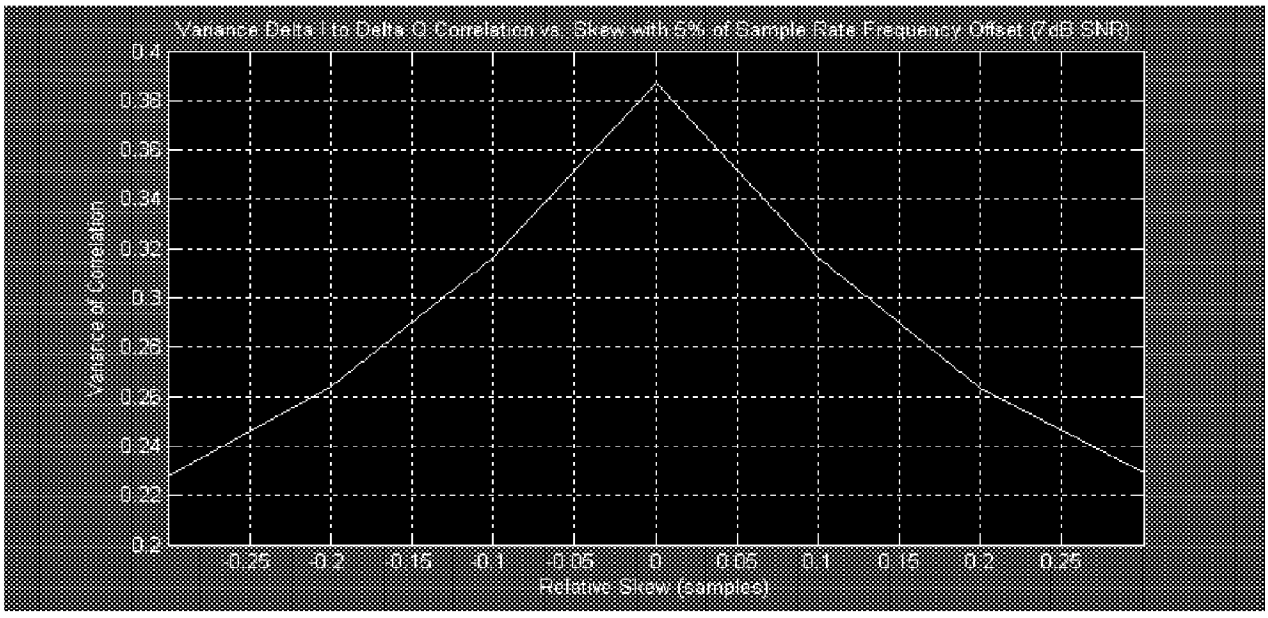
frequency offset need to be compensated prior to being able to properly evaluate the signal quality, making this option still impractical.

It turns out that if there is a certain amount of frequency offset from baseband at the ADC input then a skew between the I and Q paths generate an image signal and the amount of skew can be extracted from a correlation between the I and Q samples. This correlation turns out to be proportional to both skew and frequency offset. Unfortunately, any amount of phase imbalance in the quadrature downconverter also manifests as an I/Q correlation and, in fact, this is how it is normally removed. So it seems we have an additional problem – not only will skew degrade performance, but also, coupled with a significant frequency offset, it will also distort the I/Q phase imbalance compensation. Fortunately, there is another aspect that sets skew plus frequency offset apart from phase offset—in the presence of a time skew and a frequency offset there is a non-zero correlation between first derivatives of the I and Q samples. This correlation is exactly 0 if I and Q correlation is removed, which is typically done by the phase equalizer. This property is independent of the modulated signal, as long as the signal is "normal" and is not centered at baseband. Below is a typical result with a completely random signal, upsampled by 2 and a -7dB AWGN noise added after upsampling and a non-zero frequency offset:



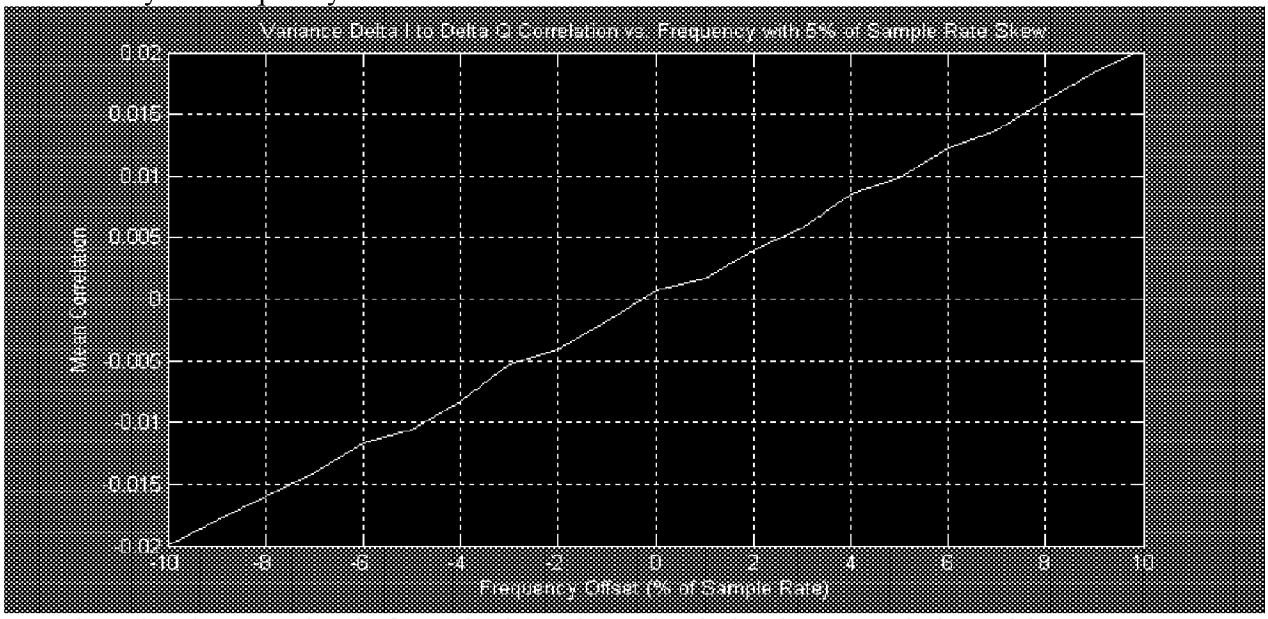
The slope of the line above depends on the input frequency offset. The variance of the samples will help determine how many samples need to be averaged for a statistically significant estimate:

[Exhibit 1-40]



Note that here UI represents one sample period. If we are dealing with a demodulator that processes 2 samples per input symbol, a UI is twice as long.

Now we need to determine what is the smallest frequency offset that we can tolerate and still get a statistically significant estimate of the skew. Let us examine the correlation of I and Q derivatives with just a the same signal, now with a fixed skew of 5% of the sample rate and vary the frequency offset:



Based on the above, a simple formula that relates the derivatives correlation with frequency offset and skew can be derived: C = 4*F*S*P, where:

C = average correlation of I and Q derivatives

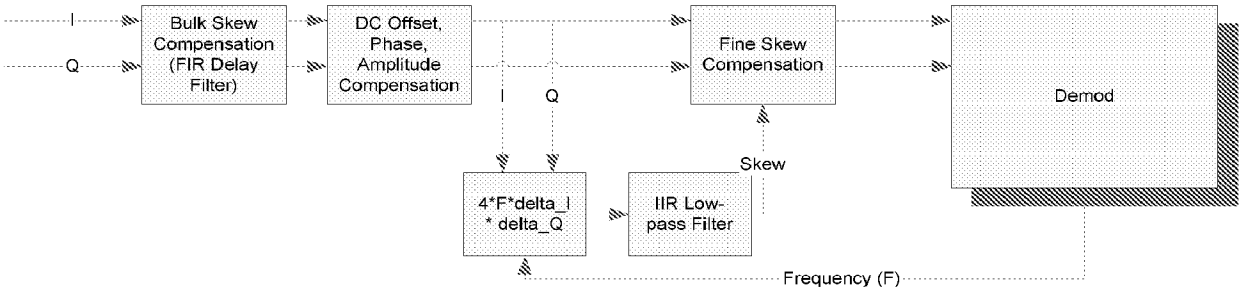
F = Frequency offset (normalized to sample rate)

[Exhibit 1-41]

S = I to Q time skew (normalized to sample rate)
P = input signal power.
This formula seems to hold true for any 2x oversampled waveform.
This allows us to determine the number of samples that needed to be averaged for a meaningful skew estimation. For example, we have a system that is at 2 samples per symbol and we want to ensure that skew is tracked to 0.5% of a symbol period (or 1% of sample period) and we can ensure that input frequency error will on average be no smaller that 0.5% of the sample rate or 1% of the symbol rate then our mean correlation should be 4*(0.005*2)*0.01=4e-4. With a worst-case of 7dB SNR we can expect worst-case variance on this measurement of 0.5. So if we want the variance of the estimate to be 25% of actual, i.e. 1e-4 then we need to average (1/1e-4)^2=1e8, or about 5 milli-seconds at 20Gsps. If we don't expect the skew to vary by more than 0.005 UI in a second, we can reduce hardware complexity by using one out of every 128 or so samples in order to come up with the estimate.

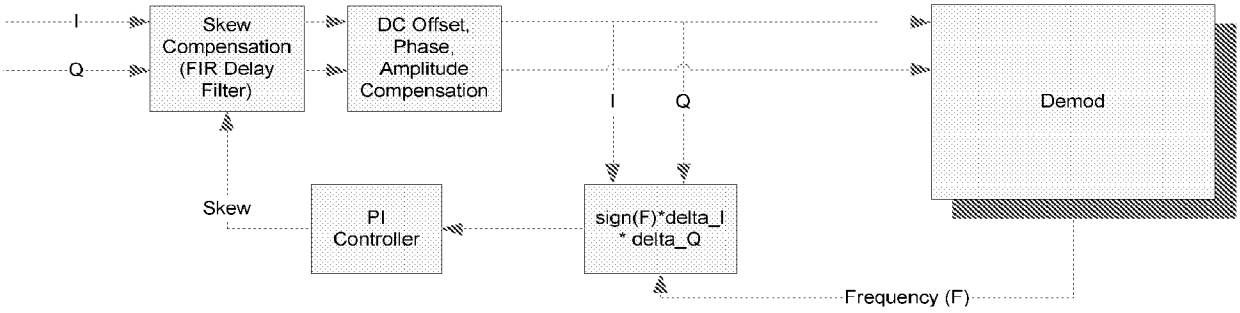
Implementation

Let us now consider several possible HW implementations of a skew compensation filter. Since we know the relationship between skew, frequency and correlation, the most straight-forward implementation is:

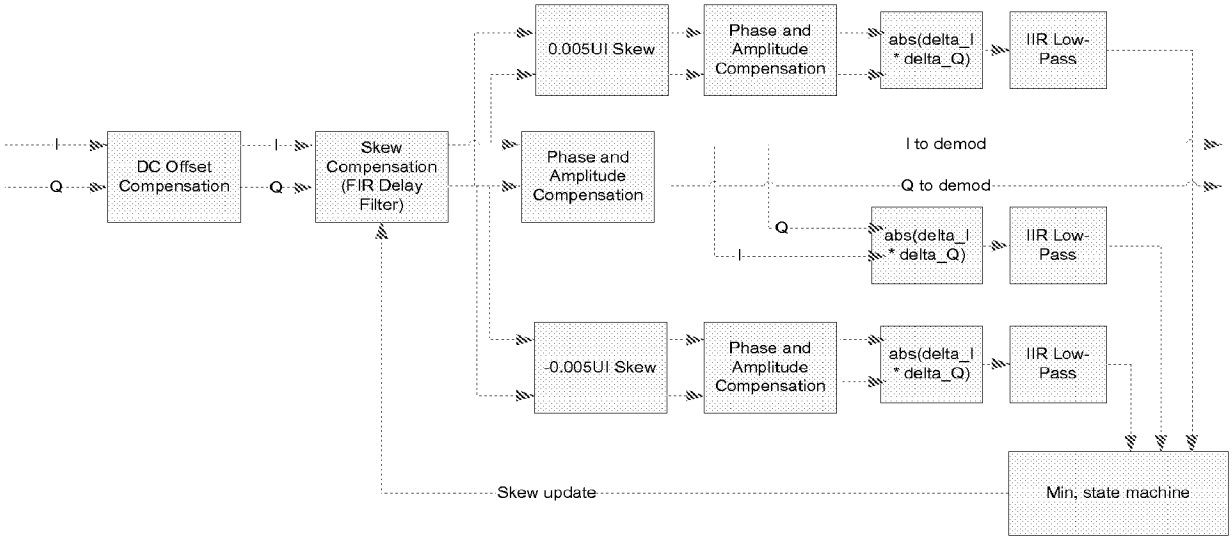


The bulk skew compensation takes out skew that is more than 0.5 UI and has to be configured during calibration. The main drawback of this implementation is that frequency has to be known, so it may be problematic if frequency offset is small and is changing, so that there is some error in the frequency value fed back from the demodulator.

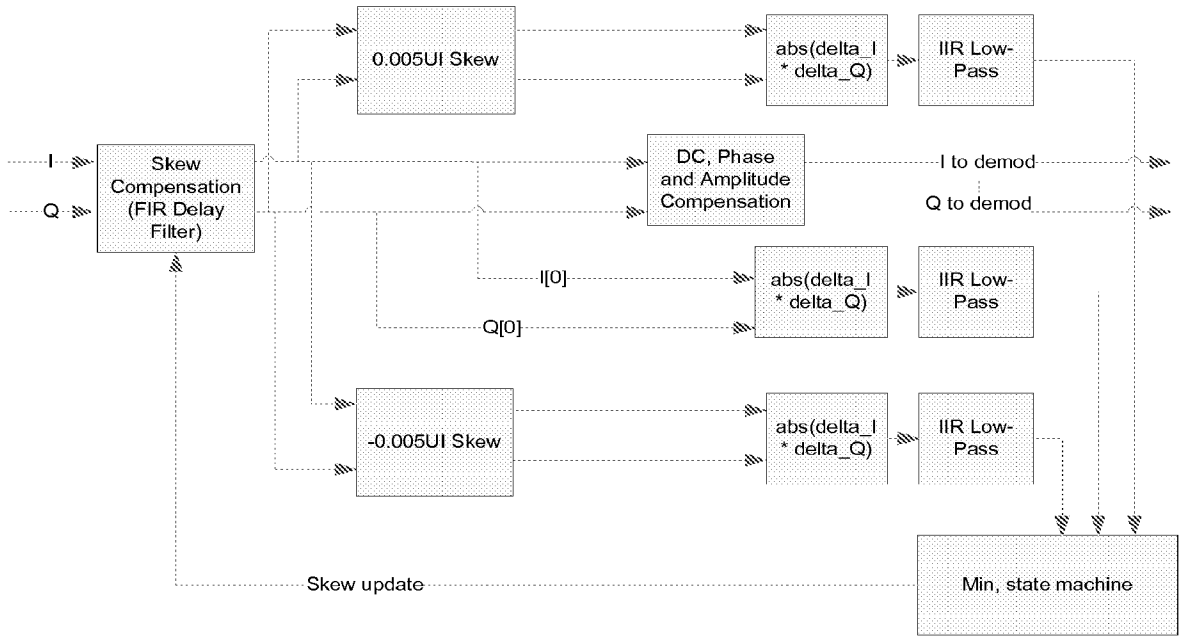
If we can assume that the demodulator is not going to provide an exact frequency value but can at least supply the sign of the frequency error we can do the following:



This implementations uses a slow feedback loop and combines bulk and fine skew compensation in one step. It still relies on some knowledge of the frequency offset. If we can assume no knowledge of frequency offset we can do the following:



In this implementation, we are simply looking for the minimum absolute value of the correlation with trials of a little additional positive and negative skew. The state machine resets the low-pass filters and waits a pre-defined amount, it then compares the three filtered correlation values and if the skewed correlations become smaller than the unskewed correlation it updates the main skew compensation filter and resets the IIR's. Finally, examining the interplay of various compensation filters, it turns out that the delta_I*delta_Q skew metric is not affected by even significant amounts of uncompensated DC, amplitude, or phase error. We can therefore simplify to the following solution:



Once again, as in the previous solution, the delta_I*delta_Q correlators can run on sub-sampled version of the samples, and the state machine updated the main skew compensation block if the center correlation is not smaller than the two +/- trials.

Multi-Layered decoding of concatenated codes

Problem Extracting maximum coding gain from hard-decision or soft-decision iterative decoding of concatenated codes

Reducing the odds of false convergence of decoding algorithms

Solution Algorithm for decoding concatenated codes in a multi-layered fashion where more likely corrections are made first to avoid creating more bit errors during initial iterations

Adapting the algorithm for high speed hard-decision TPC Decoding

Adapting the algorithm for high speed soft-decision TPC Decoding

Technical Keywords Concatenated codes, soft decoding, hard decoding

Novel This is a new technique. Can be used for performance enhancements in a variety of FEC applications.

Inventors Sameep Dave and Fan Mo

Multi-Layered decoding of concatenated codes

Decoding of powerful concatenated codes is usually an iterative process where during every iteration a pass at decoding is performed hich helps generate some extra information about the confidence in a bit being a 1 or a 0. During the initial iterations in the decoding process sometimes the decoder ends up making wrong decisions as the incoming data is very erroneous.

The proposed invention targets making the first few iterations during the decoding process more conservative by limiting the correction capability of the codes involved. This in turn would avoid the initial iterations from making things work. The full correction capacity of the code can then be unleashed on relatively cleaner data for quicker convergence and higher performance.
This technique can be applied to hard decision as well as soft decision concatenated code decoders.

Low complexity interpolator / decimator for 40 / 100 G applications

Problem Sampling rate at the Rx side in OTN systems is usually 2 + delta times the symbol rate

2x or 1x samples per symbol signaling is required for most of the Demodulator design Variable rate interpolators are very complex for 40 / 100 Gbps kind of applications / implementation

Solution Algorithm for generating a compact interpolator / decimator design optimized around the desired sampling rate to symbol rate ratio

Fixed taps filter for lower complexity

Carefully crafted connections to reduce congestion in routing for ASIC / FPGA implementation

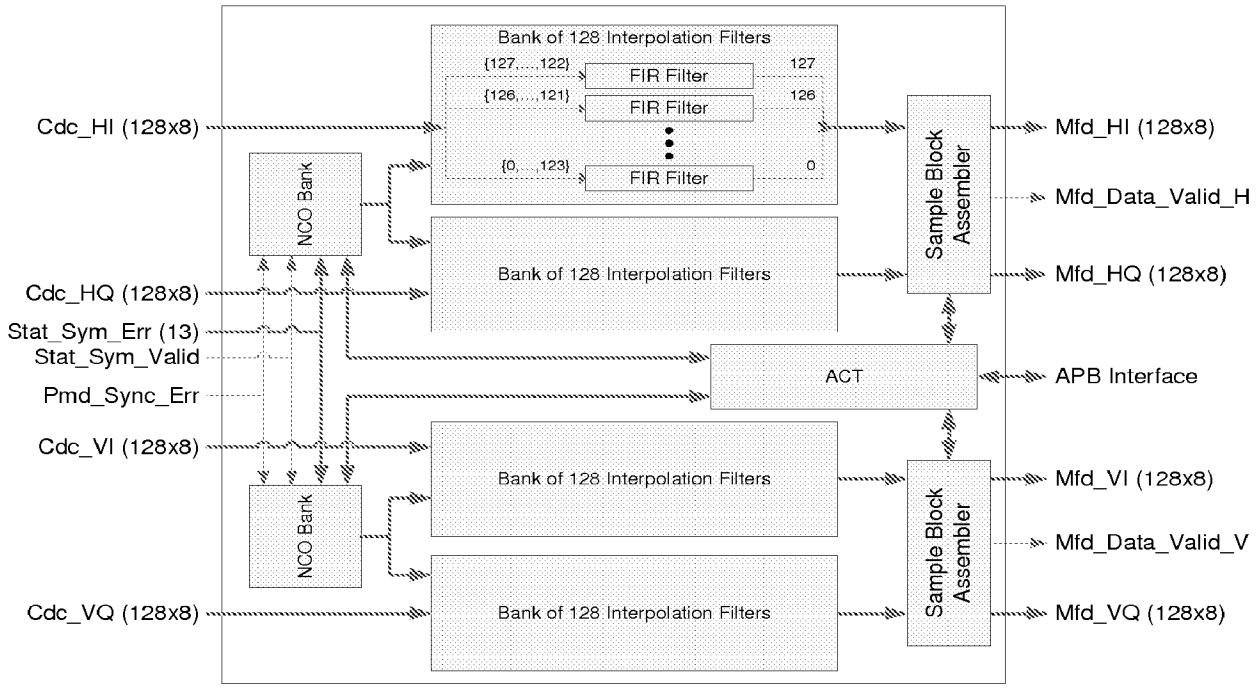
Technical Keywords Interpolator, Decimator

Novel This is a new technique. Can be used for variety of applications where range of desired sampling rate to symbol rate ratio is not huge.

Inventors Matt Nimon, Fan Mo and Bill Thesling

Low complexity interpolator / decimator

The matched filter decimator module implements an interpolation function that provides decimation from the ADC sample rate to 2x the symbol rate. Each of the four data streams has an independent bank of FIR filters with fixed coefficients. The filter coefficients implement a Raised Cosine low-pass filter with pre-determined roll-off. The symbol timing error input value fine tunes the decimation rate such that one of the two samples per symbol output is an on-time sample. The sample block assembler takes in the data samples from the filter bank and groups the samples such that valid data output from the MFD block always contains data samples output per stream. Note that valid output data is not available on each clock and the data valid output indicates when valid output data is available. The top level matched filter decimator design is shown in the figure below.



The MFD supports a single decimation rate. The decimation rate is based on the specification that the ADC sample clock will be set to 2+ times the nominal baud rate and the fact that the MFD outputs 1 or 2 samples per symbol.

Each NCO bank maintains a symbol rate NCO and generates a vector of interpolation phase values per clock. The interpolation phase values are identical for both the I and Q streams in each polarization so one NCO bank services two streams. The Pmd_Sync_Err in an input from the PMD module and is asserted if ever the data valid outputs from both polarizations are out of sync. When the Pmd_Sync_Err is asserted, the NCO banks are cleared.

The symbol error is a signed value providing for a maximum symbol timing correction capability of a certain % of the baud rate. The symbol timing error is input to the NCO bank where it is added to the nominal NCO step value to produce a corrected NCO step. The corrected NCO step value is reported as status.

There are four banks of interpolation filters in the module with each bank processing one of the data streams. Each filter bank takes in one data word of sample data and an array of interpolation phases per clock. The filter blocks filter the incoming data through the filter banks with the interpolation phase for each filter driven by the corresponding interpolation phase value. The filter bank produces 2 samples per symbol out for each data stream.

The decimation rate is controlled by a NCO so the number of output samples produced per clock is not a constant. In order to simplify data processing through the remainder of the demodulator, data samples are gathered and assembled into blocks of samples per

stream per clock by the sample block assembler. The assembly function is identical for the I and Q streams in each polarization so one assembly block services two streams.

As the ratio of the output/input samples per clock is not exact, there will be clock cycles where the matched filter decimator does not output any data. The Mfd_Data_Valid_x output is asserted only on clocks with valid output data. There is one output data valid flag per polarization (we really need only one but two facilitates the division of this function into two HLBs).

CoM based adaptive EQ tap correction

Problem In digital demodulator design adaptive Equalizers are used for recovering signal quality

Equalizer usually plays a part in the symbol timing error correction

In presence of slow residual symbol timing offset the taps of an adaptive equalizer can drift towards the edges degrading the performance

This problem is hastened in the PMD compensation equalizer for 40 / 100 Gbps OTN applications / implementation

Solution Algorithm for generating a CoM (Center of Mass) metric for the equalizer Algorithm for using the CoM metric to correct the taps without disrupting the receiver synchronization

Low complexity implementation of the algorithm for high speed receiver design

Technical Keywords Equalizer, Adaptive filter, CMA, LMS

Novel This is a new technique. Can be used for variety of applications where equalizers are used in the receiver design.

Inventors Fan Mo and Sameep Dave

CoM based adaptive EQ tap correction

In digital Demodulator designs for 40 / 100 Gbps optical systems the PMD compensation Equalizer (PMD EQ) is also a part of the symbol timing loop along with the STAT module. The EQ can interact with the symbol timing loop in such a fashion that at times the EQ filter taps on both poles can start drifting towards the edge of the filter, turning the EQ into a filter with small number of useful taps. This invention proposes CoM evaluation and correction to be performed in the PMD / PDL compensation module to make sure that if the useful EQ taps have shifted by a symbol they are moved back towards the center of the filter. To figure out if the taps have moved the CoM will be calculated as the difference between the combined tap energies of the filter taps index -7 to -1 and filter taps index 1 to 7. If the magnitude of this difference is greater than a programmable threshold the taps are instantaneously adjusted towards the center. Please note that adjustment of taps will result in addition or deletion of a symbol and needs to be accompanied by the deletion or addition (respectively) of a symbol in the data going out of the PMD EQ.

The **pmd_err_com_eval** module performs CoM related Offset and Error Calculation, Tap Offset Control as well as Tap Reset Control as shown in Figure 16. It gets the partial 20-bit CoM metrics (Com_Out_*) from the hlb_pmd_fir 4, 5, 6 and 7 and generates two

outputs that can help counter the movement of EQ filter taps (towards the edges) as shown in Figure 17.

The partial CoM metrics from the HLBs generating outputs for a particular pole are summed together before being weighed by a pole-dependent scaling factor (Z_Com_Gain_*). These gains / weights are to account for any PDL related mismatch between the two poles. The scaled results are added together and this accumulated value is used to generate couple of options for correcting the CoM. A programmable rounding / saturating oprion is made available via the Z_Com_R signal. This dictates how many LSBs versus MSBs are removed when the 12-bit output is generated.

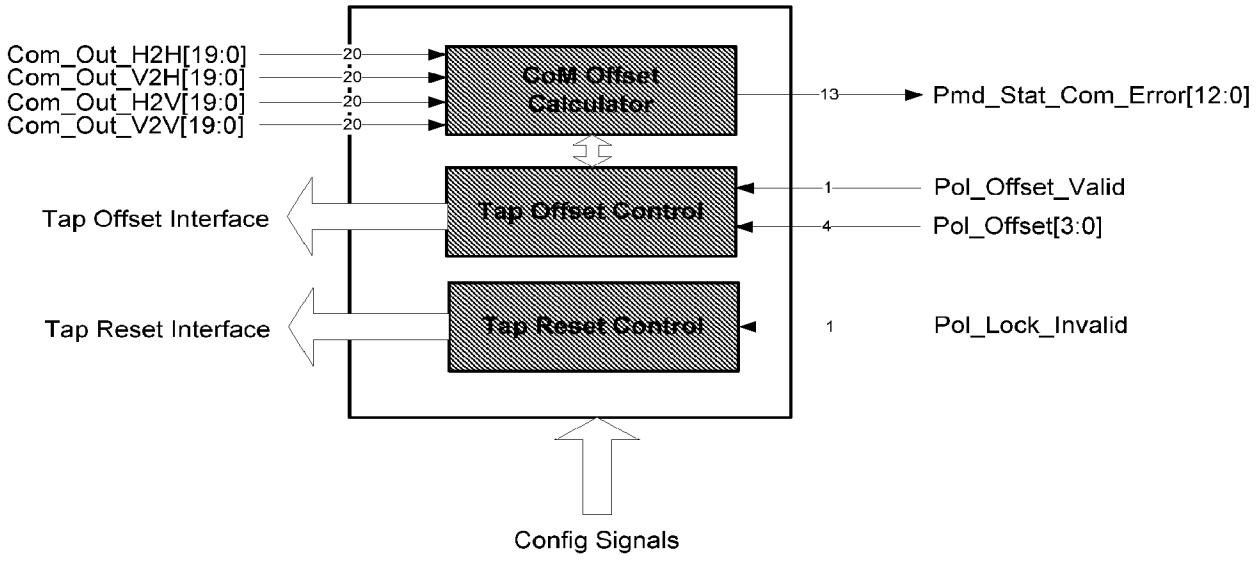


Figure 16. Operations performed by pmd_err_com_eval

The first output (preferred approach) of the CoM Error / Offset Calculator is the error signal Pmd_Stat_Com_Error[12:0] going out to the STAT module. The STAT module can use this signal in addition to its own early-late symbol timing error signal to provide an aggregate error signal to the MFD for symbol timing adjustment.

The second output (2nd option) is a 2-bit offset indicator (Com_Offset[1:0]) that goes out to the Tap Offset Control. This will result in the EQ shifting the filter taps to balance the CoM. The selection between the two options can be performed using the programmable controls shown in Figure 17. Setting the gain Z_Com_Stat_G[7:0] to 0 would turn off the first option. The sign of Z_Com_Stat_G[7:0] can control the polarity of the CoM metric ((early taps – late taps) versus (late taps – early taps)). Setting the Z_Com_Th[11:0] (unsigned) to 0xFFF (default) would turn off the second approach. Only one of the two approaches should be active at any time.

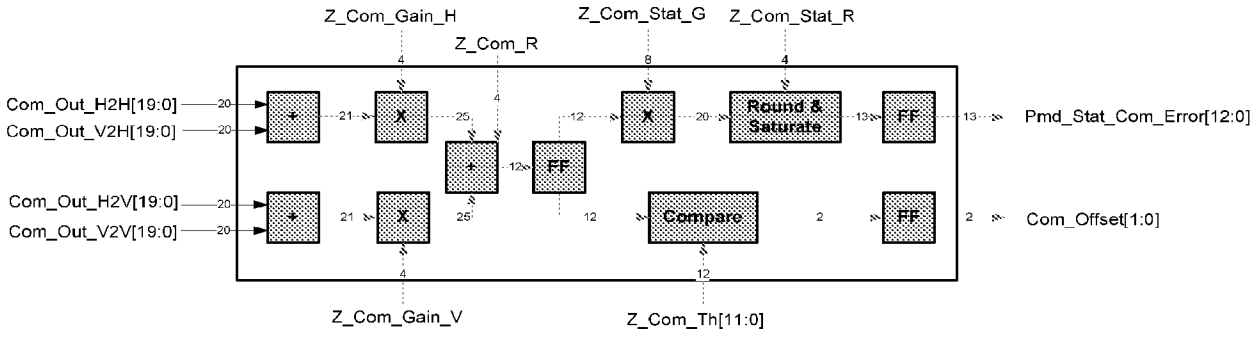


Figure 17. Operations performed for a PMD Tap update

The Tap Offset Control is responsible for regulating the shift of EQ filter taps in response to the CoM_Offset[1:0] or the polarization offset feedback coming from the FFS module. The polarization offset will have precedence over the CoM related offset. So if the polarization offset is being exercised the CoM offset should be ignored.

The design has a Tap_Offset Interface going from the **hlb_pmd_err** to the 8 **hlb_pmd_fir**. There is a unique 3-bit Tap_Offset_Indicator* for every **hlb_pmd_fir** for flexibility. The 3-bits are defined as:

- [0] : A data valid flag for offset. 0x0 (No offset required), 0x1(Offset)
- [1] : Direction of taps shift. 0x0 (New Tap [i] = Old Tap [i-2]), 0x1 (New Tap [i] = Old Tap [i+2])
- [2] : Active high blackout signal (generated by **hlb_pmd_err**) to block tap update during and right after transition

Based on the polarization or CoM offset the amount of shift to be performed will be conveyed to the **hlb_pmd_fir** using these Tap_Offset_Indicator* signals.

The CoM offset will only request shifts of one symbol (equivalent to 2 taps in the EQ filters) at a time which will require only one active high clock cycle of the data valid flag (Tap_Offset_Indicator*[0]) accompanied by the correct direction of the shift. Also the CoM offset will be the same for all the **hlb_pmd_fir.** The blackout signal (Tap_Offset_Indicator*[2]) should be kept high for 16 clock cycles to make sure the error updates generated using the older taps are flushed out of the design pipeline.

Also note that in case of Pol_Lock_Invalid being active only the V-pole needs to be reinitialized.

pmd_err_com_adjust

The **pmd_err_com_adjust** module is responsible for taking in the on-time samples (64 samples each for the 4 channels HI, HQ, VI and VQ) from the **pmd_err_out_accum**

module, making any adjustments (adding or deleting (if needed) a sample / symbol from the channels) based on the CoM offset and providing output on-time samples to the CFAT and CPR modules on a 64-sample per channel bus with either all samples valid or none on a clock cycle by clock cycle basis. A top-level block diagram of **pmd_err_com_adjust** is shown in Figure 18.

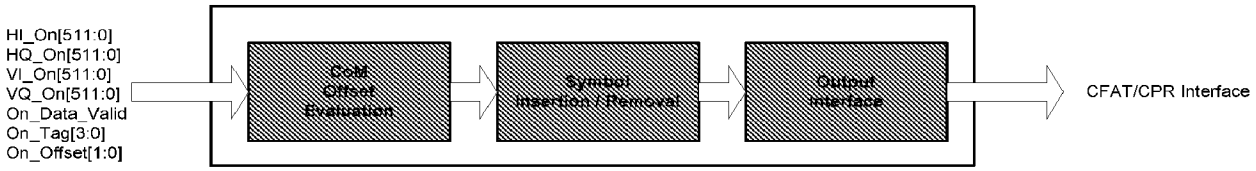


Figure 18. Operation stages inside pmd_err_com_adjust

The CoM Offset Evaluation looks at the On_Offset[1:0] signal and figures out that based on the CoM offset associated with the incoming data which of the following three actions need to be taken:

- Don't do anything (On_Offset[0] = 0 … there is no offset)
- Add a symbol (On_Offset = 2'd2)
- Remove a symbol (On_Offset = 2'd3)

Based on this decision the Symbol Insertion / Removal block will turn the incoming 64-samples per channel data bus into a 65-samples wide data bus where 63, 64 or 65 samples may be valid on any valid clock. This should just involve a simple 3-input mux for each sample. The addition / deletion of symbols will be same across the four channels (III, HQ, VI, VQ). Please note that the offset goes active for only once valid clock cycle per CoM offset event.

The Output Interface block needs to convert the 65-sample per channel wide data bus coming from the Symbol Insertion / Removal block to a 64-sample per channel wide data bus where either all or none of the samples are valid at any clock. This operation will involve a Barrel Shifter in some way / shape / form. Similar tasks are being tackled at various stages in the POLO design and so will refrain from discussing the implementation of this operation here. A common module written for project – wide use will be applied. As it turns out none of the other Barrel Shifters used elsewhere was applicable to this module so we tried to use as Designware shifter. That had issues during equivalency checking so we just created a Barrel Shifter with two multiplexor stages.

Please note that as the MFD module is performing a similar task at its output of going from a smaller number of data samples available per clock to a wider bus, it is guaranteed that we will have empty clock cycles (clock cycles where the Mfd_Data_Valid_* are 0) at least once every 32 clocks (or lesser) which will allow us to make sure that we do not overflow because of addition of extra symbols at this interface.

CoM Offset Evaluation and Symbol Insertion / Removal will be performed within a clock cycle. The Output Interface should take a minimum of 1 or maximum of 2 clock cycles.

Memory cut optimizations for decoder design

Problem Soft decision decoding designs require a lot of storage
For high speed implementation it translates into a large number of very wide but not too deep memories. Such memories are not very area efficient for ASIC implementation

Solution Modifications to TPC decoder design to repartition the distribution of data into memory to reduce the number of less efficient memory cuts.

Area and power savings for high-speed ASIC implementation

Technical Keywords Soft-decision decoder, TPC, Turbo codes

Novel This is a new technique. Can be used for any applications where TPC or other soft-decision decoders are used.

Inventors Lawrence Esker and Sameep Dave

The top-level of the SISO Full Iteration module instantiates two copies of the SISO axis-iteration as depicted in Figure 1. It also includes a bypass multiplexer and pipeline flops to help maintain timing closure. The top-level module will be provided in unencrypted form to allow full review by Ciena to tweak their system test and power reduction strategies.

The bypass logic enables a static selection of power reduction versus decoder BER performance system tradeoff. When bypass is enabled, the input ports will direct route to the output ports and a power-down control signal (for use as a gated clock enable via Synopsys Power Compiler) is generated.

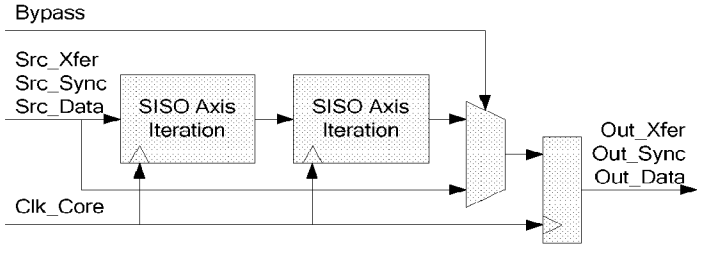


Figure 1. SISO Full Iteration with Bypass

A notional view of the SISO Axis Iteration is depicted in Figure 2.

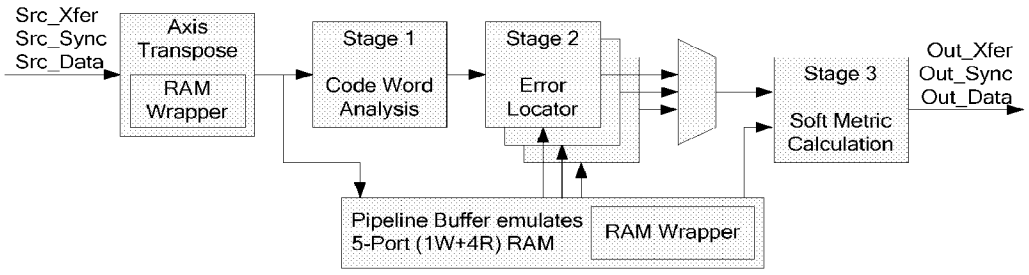


Figure 2. SISO Axis Iteration Notional View

The axis transpose RAM processes data at 256 elements per clock cycle. It simply swaps the rows and columns of the TPC such that consecutive iterations of the decoder can process the complete TPC block using replicated design for each axis iteration. The Axis Transpose contains two single port RAM arranged in a ping-pong, such that a block can be read in and another processed out simultaneously. The physical RAM implementation within the RAM Wrapper will break this up into multiple copies of narrower RAM as determined by the ASIC library.

Stages 1 and 3 of the decoder processes data at multiple elements per clock cycle. There are multiple parallel running copies of the decoder stages and pipeline buffer RAM assembly. Overall, the decoder processes a large number of elements per clock, required to meet the desired performance throughput at the target clock speed.

The decoder itself is highly pipelined such that while Stage 1 is analyzing a row of the TPC, stage 2 is examining the results of the previous row's analysis to locate errors. Stage 3 is computing soft metrics for an earlier row. As each row must be processed in a fixed number of clocks, there is not enough time for stage 2 to do its work. Multiple copies of stage 2 are staggered in time to enable extra clock cycles of error locating clocks.

To do their work, stage 2 and 3 require random access to the original input data that stage 1 had analyzed. As a result, a 5-port RAM must be emulated. This was accomplished in the design using five copies of single port RAM and multiplexers to route address and data to the appropriate RAM. Single port RAM is usually ideal for ASIC as it typically consumes the least area per bit.

While analyzing changes that would need to be made to the decoder for the high speed application, we discovered it is possible to alter the Pipeline Buffer topology from its original design.

- Current -- A single decoder's row pipeline buffer RAM is 5 copies of 14 words deep by 160 bits wide single port RAM.
- Alternate -- Stage 2 does not require access to all 160 bits. The 5-port emulation can be reduced to 80 bits wide. In addition, there is 1 copy of 80 words deep by 80 bits wide two-port RAM.

Due to the parallelism of the design, the per row RAM requirements are multiplied by 16 for a axis iteration and by 8 again for the complete design.

High speed SDFEC / TPC decoder design complexity is dictated by the memory as for highly parallel processing lots of soft-information needs the be written to / read out from memory on ever clock of data processing. Re-evaluating e memory cuts in the design to split up parts of information that need to be actively accesses versus parts that are rarely used and can be stowed away together helps drive the overall complexity as well as power consumption for the decoder design.

PMD Equalizer reseeding based on initial pole offset

Problem In optical fiber communications PMD (polarization mode dispersion) is a critical impairment.

Equalizer is required on the receiver side to track / correct PMD.

Big polarization offset during acquisition can cause the equalizer taps to converge such that when the PMD recovers to nominal values the taps are not centered leading to degraded performance.

Solution Algorithm for creating feedback from the framer / decoder to PMD equalizer to help shift the filter taps in accordance with the polarization offset during acquisition.

Ensures tap seeding such that during nominal PMD the equalizer can extract optimal performance

Technical Keywords PMD, Equalizer, Dual pole, PMQPSK, PM-DQPSK

Novel This is a new technique applicable to dual pole fiber communications.

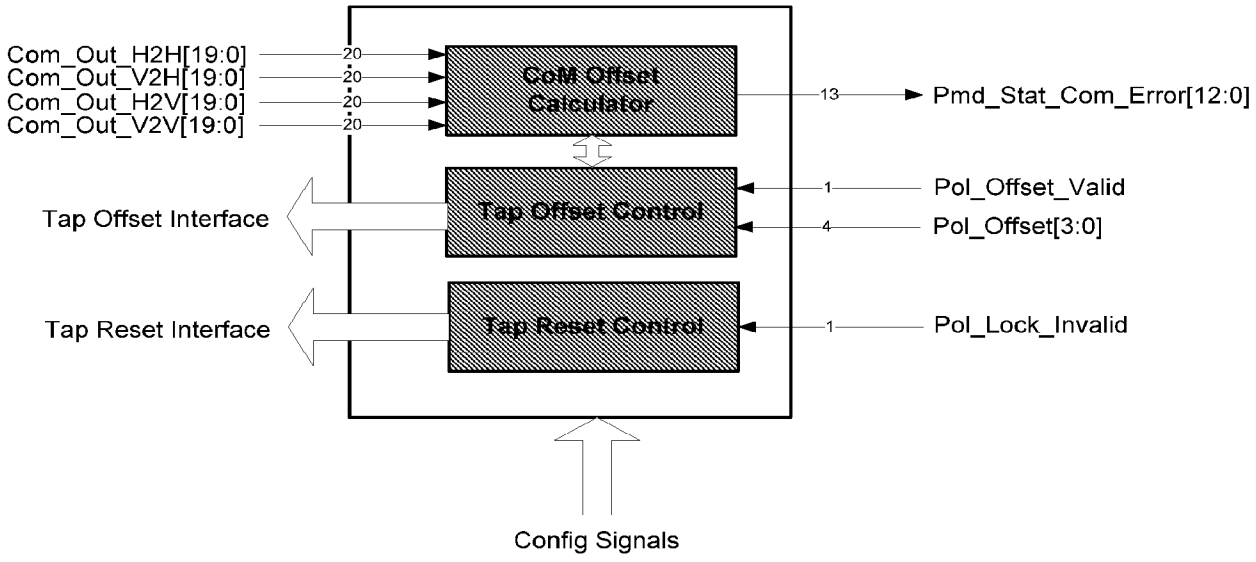
Inventors Fan Mo and Sameep Dave

PMD Equalizer reseeding based on initial pole offset

The PMD/PDL compensation / equalizer module utilizes adaptive equalization to compensate for the cross polarization interference, IQ channel interference, adjacent symbol interference introduced by PMD and PDL in optical channel and other residual impairments (like residual CD).

At initial acquisition stage if the UW detector / FFS detects a timing offset between the two poles it will convey that offset value to the EQ so that the filter taps can be re-initialized or shifted to compensate for the offset. This offset is performed in a balanced fashion between the filter taps generating the outputs for the two poles to make sure sufficient taps are available towards the edge of the filter.

If such compensation is not performed the EQ might converge such that during normal operation the higher weight taps (on one of the poles at any time) get skewed towards the edge of the filter essentially turning the EQ into a filter with small number of useful (relatively bigger value) taps.



The design has a Tap_Offset Interface going from the **hlb_pmd_err** to the 8 **hlb_pmd_fir**. There is a unique 3-bit Tap_Offset_Indicator* for every **hlb_pmd_fir** for flexibility. The 3-bits are defined as:

- [0] : A data valid flag for offset. 0x0 (No offset required), 0x1(Offset)
- [1] : Direction of taps shift. 0x0 (New Tap [i] = Old Tap [i-2]), 0x1 (New Tap [i] = Old Tap [i+2])
- [2] : Active high blackout signal (generated by **hlb_pmd_err**) to block tap update during and right after transition

The Polarization offset may request shifts of upto +/- 3 (could be any desired number) symbols at a time. And it will need different amounts of correction on the **hlb_pmd_fir** responsible for the H-pole (0, 2, 4, 6) output versus V-pole output (1, 3, 5, 7) as shown in **Error! Reference source not found.**. The number of active high clock cycle of the data valid flag (Tap_Offset_Indicator*[0]) required for a set of **hlb_pmd_fir** HLBs will be equal to the number of symbol shifts required for its taps. Because of taps needing to cross HLB boundaries during the shift the data valid should be sent as multiple 1 clock cycle wide pulses, once every 4 clock cycles. This will give enough time for the end taps from one HLB to transferred to the other HLB and be apart of the updated taps. The blackout signal (Tap_Offset_Indicator*[2]) should be kept high for 16 clock cycles to make sure the error updates generated using the older taps are flushed out of the design pipeline. Please note that Pol_Offset being positive means H pole is leading the V pol.

Table 1. Desired tap offsets based on Pol_Offset[3:0] / V-II offset from FFS

V - H offset	New Tap(i) for generating H	New Tap(i) for generating V
-6	Old Tap[i-6]	Old Tap[i+6]
-5	Old Tap[i-4]	Old Tap[i+6]
-4	Old Tap[i-4]	Old Tap[i+4]
-3	Old Tap[i-2]	Old Tap[i+4]
-2	Old Tap[i-2]	Old Tap[i+2]
-1	Old Tap[i]	Old Tap[i+2]
0	Old Tap[i]	Old Tap[i]
1	Old Tap[i+2]	Old Tap[i]
2	Old Tap[i+2]	Old Tap[i-2]
3	Old Tap[i+4]	Old Tap[i-2]
4	Old Tap[i+4]	Old Tap[i-4]
5	Old Tap[i+4]	Old Tap[i-4]
6	Old Tap[i+6]	Old Tap[i-6]

One trial per clock architecture for high speed TPC Decoding

Problem For very high speed TPC decoder designs high degree of parallelism is needed. The most complex processing stage in the TPC decoder is the processing stage where multiple trials / attempts at decoding are made. Decoding trials need to be spaced at t clocks where t is the correction capacity of the component BCH code. Requires duplicating the whole trial processing stage.

Solution Architecture change where selective replication of a small portion of the trial processing stage can allow to launch one trial per clock. Leads to significant reduction of overall decoder complexity.

Technical Keywords 100 G, TPC, Decoder, Chase

Novel This is a new architecture that can avoid needing multiple copies of the most complex section of the decoder design for high speed applications thus reducing complexity.

Inventors Sameep Dave and Lawrence Esker

One trial per clock architecture for high speed TPC Decoding

The top-level of the SISO Full Iteration module instantiates two copies of the SISO axis-iteration as depicted in Figure 1. It also includes a bypass multiplexer and pipeline flops to help maintain timing closure. The top-level module will be provided in unencrypted form to allow full review by Ciena to tweak their system test and power reduction strategies.

The bypass logic enables a static selection of power reduction versus decoder BER performance system tradeoff. When bypass is enabled, the input ports will direct route to the output ports and a power-down control signal (for use as a gated clock enable via Synopsys Power Compiler) is generated.

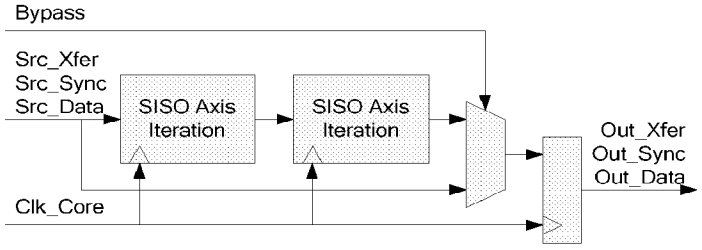


Figure 1. SISO Full Iteration with Bypass

A notional view of the SISO Axis Iteration is depicted in Figure 2.

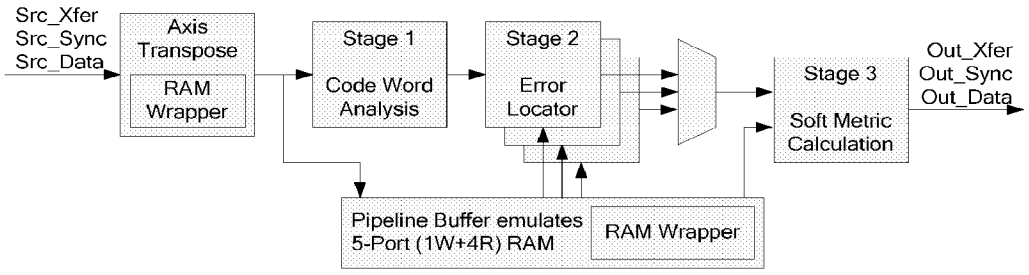


Figure 2. SISO Axis Iteration Notional View

The axis transpose RAM processes data at 256 elements per clock cycle. It simply swaps the rows and columns of the TPC such that consecutive iterations of the decoder can process the complete TPC block using replicated design for each axis iteration. The Axis Transpose contains two single port RAM arranged in a ping-pong, such that a block can be read in and another processed out simultaneously. The physical RAM implementation within the RAM Wrapper will break this up into multiple copies of narrower RAM as determined by the ASIC library.

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Stage 2 is the most computationally intensive stage in the decoding process and needing multiple copies of this stage hugely impacts the overall decoder complexity. This invention proposes replication of just few pieces inside the stage 2 such that instead of every trial taking a few clock cycles, one trial can be launched per clock. This can drastically reduce the number of copies of the stage 2 of the decoding process for high speed applications leading to major savings in overall complexity.

One of the main reasons why trials take multiple clock cycles is that if a given trial finds a few error locations the logic has to access the soft information data from memory for these locations one by one to evaluate the effectiveness of the trial. Instead of doing this one-by-one for the various error locations if a multi-port memory is employed the information can be gathered within a clock cycle allowing the decoding to proceed at one trial per cycle.

Acronym/Abbreviation	Definition
ACT	Automatic Configuration Tool
ASIC	Application Specific Integrated Circuit
BER	Bit Error Rate
BPE	Block Phase Estimator
CD	Chromatic Dispersion
CDC	CD Compensation
CFAT	Carrier Frequency Acquisition and Tracking
CPR	Carrier Phase Recovery
DFT	Discrete Fourier Transform
DWDM	Dense Wavelength Division Multiplexing
ENOB	Effective Number Of Bits
EQ	Equalizer
FEC	Forward Error Correction
FFS	FEC Frame Synchronizer
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
HDFEC	Hard Decision FEC
HI	I channel of Horizontal polarization
HQ	Q channel of Horizontal polarization
IFFT	Inverse FFT
IIR	Infinite Impulse Response
MFD	Matched Filter Decimator

NA	Not Applicable
NCO	Numerically Controlled Oscillator
PI	Proportional-Integral
PMD	Polarization Mode Dispersion
PP	Physical Partitions
QEF	Quadrature Error Filter
QPSK	Quadrature Phase Shift Keying
RLM	RTL Layout Macro
STAT	Symbol Timing Acquisition and Tracking
TBD	To Be Decided
TBR	To Be Reviewed
UW	Unique Word
UWH	Unique word inserted in the horizontal polarization
UWV	Unique word inserted in the vertical polarization
VI	I channel of Vertical polarization
VQ	Q channel of Vertical polarization

WHAT IS CLAIMED IS:

1. An apparatus and a method for high rate optical communication as described in the specification and figures.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	High Rate Optical Communication
First Named Inventor/Applicant Name:	Sameep Dave
Filer:	Charles Nicholas Pateros/Stacy Nguyen
Attorney Docket Number:	ECC-0452-US

Filed as Large Entity

Provisional Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Provisional application filing	1005	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**220**

Electronic Acknowledgement Receipt

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International Application Number:	
Confirmation Number:	5581
Title of Invention:	High Rate Optical Communication
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	31864
Filer:	Charles Nicholas Pateros
Filer Authorized By:	
Attorney Docket Number:	ECC-0452-US
Receipt Date:	22-JAN-2011
Filing Date:	
Time Stamp:	11:19:23
Application Type:	Provisional

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Payment Type	Credit Card
Payment was successfully received in RAM	$220
RAM confirmation Number	8480
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

[Exhibit 1-66]

1	Provisional Cover Sheet (SB16)	FiledECC-0452ProvisionalSB.pdf	1060271 beb77e1e0613ca193fb87494bd6668a0567b0b69	no	4
Warnings:					
Information:					
2	Specification	FiledECC-0452-US-prov-app110121-1132a.pdf	523364 ffbc6a5b4ebffc9a6c3bba814519307d0d184575	no	55
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	28905 c9a12986eee7d6adb0ef7cc919ea5ba4863b1ed2	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1612540		

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New International Application Filed with the USPTO as a Receiving Office

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